
TECHNICAL MANUAL

GS MAINTENANCE MANUAL

TEST SET, CONVERTER

SUBASSEMBLY-VIDEO

CONVERTER AN/AAM-35

(NSN 6625-00-403-1064)

This copy is a reprint which includes current pages from Changes 1 through 3

HEADQUARTERS, DEPARTMENT OF THE ARMY

NOVEMBER 1970

WARNING

DEATH or SERIOUS INJURY may result from HAZARDS in this equipment. READ and OBSERVE the following WARNINGS.

WARNING

DEATH or SERIOUS INJURY may result from contact with 115-VAC, 400-Hz, 3-PHASE power existing within this equipment.

CHANGE NO. 3

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, DC, 31 May 1983

General Support Maintenance Manual
Test Set, Converter Subassembly-Video Converter
AN/AAM-35 (NSN 6625-00-403-1064)
Change No. 3 is current as of February 1983

TM 11-6625-1824-40,19 November 1970, is changed as follows:

1. Added or revised material is indicated by a vertical bar in the margin of the page. Where an entire chapter, section, or illustration is added or revised, the vertical bar is placed opposite the title or identification number. Remove old pages and insert new pages as indicated below.

Remove pages	*pages*
1-1	1-1/(1-2 blank)
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FO-4[1]	FO-4[1]
FO-7[4]	FO-7'[4]

2. File this change sheet in the front of the publication.

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HEADQUARTERS
DEPARTMENT OF THE ARMY
WASHINGTON, DC, *19 November 1970*

GENERAL SUPPORT MAINTENANCE MANUAL
TEST SET, CONVERTER SUBASSEMBLY-VIDEO CONVERTER
AN/AAM-35
(NSN 6625-00-403-1064)

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CHAPTER 1

INTRODUCTION

1-1. Scope of Manual

a. This manual contains functioning of equipment and general support maintenance for Test Set, Converter Subassembly-Video Converter AN/AAM-35. General support maintenance includes troubleshooting, removal and replacement, adjustment and alignment, repair and general support testing.

b. Operator and organizational maintenance procedures are contained in Technical Manual (TM) 11-6625-1824-12.

1-2. Consolidated Index of Army Publications and Blank Forms

Refer to the latest issue of DA Pam 310-1 to determine whether there are new editions, changes or additional publications pertaining to the equipment.

NOTE

Applicable forms and records are covered in TM 11-6625-1824-12.

1-3. Reporting Errors and Recommending Improvements

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter or DA Form 2028 (Recommended Changes to Publications and Blank Forms) directly to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: DRSEL-ME-MP, Fort Monmouth, NJ 07703. In either case, a reply will be furnished directly to you.

1-3.1. Reporting Equipment Improvement Recommendations (EIR)

If your AN/AAM-35 needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design. Put it on an SF 368 (Quality Deficiency Report). Mail it to Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: DRSEL-ME-MP, Fort Monmouth, NJ 07703. Well send you a reply.

1-4. Reference Designations

Reference designations for major components of Test Set, Converter Subassembly-Video Converter AN/ AAM-35 are listed in TM 11-6625-1824-12.

CHAPTER 2

FUNCTIONING OF EQUIPMENT

Section I. BLOCK DIAGRAM DISCUSSION

2-1. Overall Function

The converter test set performs a bench test of either Converter Subassembly MX-8358/AAS24 (converter subassembly) or Video Converter CV-2666/AAS-24 (video converter). The converter subassembly is tested for write video, write horizontal sweep, write vertical sweep, read vertical sweep, read horizontal sync, and hot target marking by waveform analysis; power supplies by dvm measurement; and bit logic by input simulation. The video converter is tested for write video, write horizontal deflection current, write vertical deflection current, hot target marking, read horizontal current sample, and read video by waveform analysis; focus, tube burnspot, and alignment show up as oscilloscope performance. Limited calibration of the converter subassembly and video converter electronics is possible with the converter test set.

2-2. Block Diagram

(fig. FO-2, FO-3)

a. Ac Power Distribution. The 115-vac, 400-Hz, 3-phase primary power is applied through the filter to circuit breaker CB2. From CB2 the power is applied to the contacts of standby relay 1A1K1 and phase sensing relay 1A1K5. The proper phase rotation (A, B, C) causes 1A1K5 to operate and complete a path for a monitored +5vdc signal to power control 1A1A6. When standby relay 1A1K1 operates, ac power is applied to converter test set, unit 2, to ELAPSED TIME meter 1A1M1, and to power transformer 1A1T1 where the ac voltage is stepped up and down, applied to 1A1A1, 1A1A2, 1A1A3, 1A1A5 and 2A1A14 to be rectified and filtered to supply dc power required for operation of the converter test set. When operate relay 1A1K2 operates, 115-vac, 400-Hz, 3-phase power is applied to the unit under test.

b. Dc Power Distribution. The 28-vdc power is applied through the filter, through CB1, to the power mode switch and to the contacts of standby relay 1A1K1. Setting the power mode switch to STBY applies 28 vdc to light the STBY lamp and to operate standby relay 1A1K1 causing it to apply 28 vdc to the contacts of operate relay 1A1K2. Setting the power mode switch to OPR extinguishes the STBY lamp, causes operate relay 1A1K2 to operate, lights the OPR lamp and applies 28 vdc to the unit under test.

c. Power Inputs. Input power of +5 vdc, -15 vdc, and 28 vdc is shown on the block diagram as a matter of familiarization. Signal inputs and outputs are the prime consideration in this discussion.

d. Test Points. Many test points are provided on the converter test set to sample signals from the unit under test and converter test set signals. Some of these test points are shown on the block diagram.

e. Load Boards 1A1A11 and 1A1A12. These boards are composed of resistors which provide loads for input signals. Inputs to load board 1A1A11 are sweeps, syncs, samples, blanking and video from the unit under test. Inputs to load board 1A1A12 are hot target marker, read vertical step and display vertical step from the unit under test. There are no outputs as such from the load boards. The input signals are applied through resistors for attenuation or impedance matching to go to test points or be sampled in the converter test set.

f. Test Voltage. The test voltages from the unit under test are made accessible at test points in unit 1 and are applied to loads located in unit 2.

g. Power Transformer, 1A1T1. The 115-vac, 400-Hz, 3-phase power applied to power transformer 1A1T1 is stepped up and down and the outputs applied to the respective dc power supplies. The ELAPSED TIME meter 1A1M1 is driven by phase A input to the power transformer.

h. Dc Power Supplies. The 250-vdc power supply 1A1A3, the 150-vdc power supply 1A1A4, the 6.3-vdc power supply 1A1A5, and the 15-vdc power supply 2A1A14 each apply their output through a heatsink to accomplish heat dissipation. The +5-vdc integrated circuit power supply (1A1A2) does not apply its output through a heatsink. Each power supply, except the 6.3 vdc, applies its output to power control 1A1A6 for monitoring.

i. Filter Assembly, 1A1A15. The inputs and outputs of this unit are 115 vac, 400 Hz, 3 phase and 28 vdc. The filter materially decreases the effect of any incoming transient which may tend to influence the proper operation of a printed circuit board or the converter test set.

j. Cs-vc Simulator, 1A1A7. The input to simulator 1A1A7 is 100 kHz from signal generator 2A1A1 from which the outputs of simulated video to video interface 1A1A8 and simulated video gate to sync interface 1A1A9 are developed.

k. Video Interface, 1A1A8. The inputs to video interface 1AlA8 are video 1 and video 2 from the unit under test or the simulated video from cs-vc simulator 1A1A7. Outputs are video 1 and video 2 which go to converter test set unit 2 to write video amplifier 2A1A6.

l. Power Mode Switch. The power mode switch controls the application of power for the standby (STBY) 6perate (OPR), and RESET modes of operation of the converter test set. The STBY lamp and OPR lamp light as indications of the mode of operation.

m. Phase Sensing Relay, 1A1K5. Phase sensing relay 1A1K5 monitors the 3-phase ac and if all phases are in correct sequence (A, B, C) operates to provide a path for + 5 vdc to power control 1A1A6.

n. *Power control*, 1A1A6 monitors the 5- 250-, 150, 15- and -15-vdc power supply outputs. Should any of these monitored inputs exceed upper or lower tolerance, power control 1A1A6 removes the ground to restore operate relay 1A1K2 to remove power from the unit under test, extinguish the OPR lamp and light the FAIL lamp. To reactivate the converter test set, the power mode switch is set to RESET and released. The power mode switch is spring loaded, so it returns to the OPR position. If all inputs to power control 1A1A6 are in tolerance, the converter test set remains in the OPR mode as indicated by the lighted OPR lamp. The phase sensing relay 1A1K5 is in the operate condition as long as the 115-vac, 400-Hz, 8-phase input to the 1A1K5 continues to have the proper phase rotation. If the input fails in this respect, phase sensing relay 1A1K5 opens to remove the +5-vdc input to power control 1A1A6. If power control 1A1A6 senses an out of tolerance condition, it causes the FAIL lamp to light, the OPR lamp to extinguish and the STBY lamp to light. The converter test set is reactivated by setting the power mode switch to RESET, providing that the power control inputs are in tolerance.

o. Hot Target and Slew Voltage Generator, 1A1A10. The inputs to hot target and slew voltage generator 1A1A10 is video gate from sync interface 1A1A9 and slew reference voltage from the unit under test. Outputs are hot target and slew voltages to the unit under test.

p. Sync Interface, 1A1A9. The inputs to sync interface 1A1A9 are the simulated video gate from cs-vc simulator 1A1A7, which becomes video gate and the hot target signals from hot target and slew voltage generator 1A1A10 which becomes hot target. The outputs other than above are velocity over height and velocity over height field of view.

q. Relays 2A1K1, 2A1K2, and 2A1K3. Transfer relays 2A1K1, 2A1K2 and 2A1K3 provide paths for power applied from converter test set unit 1 to the unit under test. These relays operate when operate relay 1A1K2 in unit 1 operates unless a unit under test is not present or there is a bad connection. In either case a safety interlock prevents operation of the relays and application of power to the unit under test.

r. 15-vdc Power Supply, 2A1A14. The inputs to the 15-vdc power supply 2A1A14 are 20.9-vac, 3-phase power. The unregulated dc and drive for the series regulator is applied to heatsink 2A1A15. One other input to the heatsink is +150 vdc. Outputs of 2A1A15 are 100 vdc to the ALIGNMENT switch and regulated 15 vdc to unit 1.

s. Switches: ALIGNMENT, 2A1S10; SLEW, 2A1S7; FIELD OF VIEW, 2A1S6.

(1) ALIGNMENT switch 2A1S10 selects signals to be applied to the unit under test for focus testing.

(2) SLEW switch 2A1S7 in conjunction with FIELD OF VIEW switch 2A1S6 selects the slew voltage to be applied to write horizontal slew and for fov adder 2A1A5.

(3) FIELD OF VIEW switch 2A1S6 also selects the fov defeat signal to be applied to write horizontal slew and fov adder 2A1A5.

(4) VERT SWEEP, 2A1S1 and LRU, 2A1S9 select various signals to be monitored at the associated test points.

t. Dither Generator, 2A1A11. Inputs to dither generator 2A1A11 are v/h from sync interface 1A1A9, chopper drive from auxiliary deflection Logic 2A1A10, and dither blanking from the unit under test. The output is dither to the unit under test.

u. Auxiliary Deflection Logic, 2A1A10. The input to auxiliary deflection logic is the v/h signal from sync interface 1A1A9. Outputs are chopper drive to dither generator 2A1A11 and select or chop to write video amplifier 2A1A6.

v. Write-Video Amplifier, 2A1A6. Inputs to write-video amplifier 2A1A6 are video and calibration indicator video from video interface 1A1A8, and select or chop from auxiliary deflection logic 2A1A10. The output is write video to the unit under test.

w. Sweep and Blanking, 2A2A12. Inputs to sweep and blanking 2A2A12 are horizontal and vertical sync signals from sync generator 2A1A2. Outputs are blanking to storage tube protect, loads and video amplifier 2A1A13 and vertical and horizontal sweeps to test points.

x. Storage Tube Protect, Loads and Video Amplifier, 2A1A13. Inputs to storage tube protect, loads and video amplifier 2A1A13, are blanking pulse from sweep and blanking 2A2A12, read video from the unit under test, and 28 vdc. Outputs are the 28 vdc as storage tube protect to the unit under test and read video amplified and blanked to test point Z OSCP.

y. V/h Clock Pulse Generator, 2A1A7. Inputs to the v/h clock pulse generator 2A1A7 are the 4095 count from write vertical sweep generator 2A1A8, v/h from sync interface 1A1A9 and vertical sync from sync generator 2A1A2. Outputs are clock pulse to write vertical sweep generator 2A1A2. Outputs are clock pulse to write vertical sweep generator 2A1A8 and write vertical blanking to write vertical sweep generator 2A1A8 and write horizontal slew and fov adder 2A1A5.

z. Write Vertical Sweep Generator, 2A1A8. Inputs to the write vertical sweep generator 2A1A8, are write vertical blanking and clock pulse from v/h clock pulse generator 2A1A7. Outputs are write vertical ramp to the unit under test and erase vertical generator 2A1A9, and 4095 count to v/h clock pulse generator 2A1A7.

aa. Load relays 2A1K4 and 2A1K5. Load relays 2A1K4 and 2A1K5 provide loads for the -15-, 15-, 5-, 150-, 250- and 6.3-vdc power supplies in the unit under test. These relays operate when a signal is applied from unit 1.

ab. Signal Generator, 2A1A1. The inputs to signal generator 2A1A1 are frame hold from TUBE PROTECT/FRAME HOLD, 2A1S5 and video gate from sync interface 1A1A9. Outputs are frame hold and gated video to the unit under test and 100 kHz to sync generator 2A1A2.

ac. Sync Generator, 2A1A2. The input to sync generator 2A1A2 is the 100 kHz from signal generator 2A1A1. The vertical sync output goes to the unit under test, to v/h clock-pulse generator 2A1A7, read vertical sweep generator 2A1A3 and horizontal and vertical sync to sweep and blanking 2A2A12. The read horizontal sync goes to the unit under test.

ad. Write Horizontal Sweep Generator, 2A1A4. The write horizontal sweep generator 2A1A4 has one input, video gate. The outputs are slew voltage to SLEW, 2A1S7, write horizontal sweep to write horizontal slew and for fov 2A1A5, and erase retrace to erase vertical sweep generator 2A1A9.

ae. Read Vertical Sweep Generator, 2A1A3. The read vertical sweep generator 2A1A3 has one input to read vertical sync from sync generator 2A1A2. There is one output of read vertical sweep to the unit under test.

af. Write Horizontal Slew and Fov Adder, 2A1A5. The inputs to write horizontal slew and fov adder are video gate from sync interface 1A1A9, write horizontal sweep and slew voltage from write horizontal sweep generator 2A1A4, field of view from 2A1S6 and write vertical blanking from v/h clock-pulse generator 2A1A7. Outputs are write horizontal sweep and write composite blanking to the unit under test.

ag. Erase Vertical Sweep Generator, 2A1A9. Inputs to the erase vertical sweep generator are erase retrace from write horizontal sweep generator 2A1A4, video gate from sync interface 1A1A9, and write vertical ramp from write vertical sweep generator 2A1A8. The output is write vertical composite sweep to the unit under test.

Section II. CIRCUIT DISCUSSION

2-3. Equipment Interconnection
(fig. 2-1)

A complete converter test set is formed by connecting the equipment as shown in figure 2-1.

2-4. Circuit Functioning
(fig. FO-4 and FO-5)

a. Ac Power Distribution.

(1) The 115-vac, 400-Hz, 3-phase power enters the converter test set through 1A1J2-A, B, C, and D. This input is applied to filter assembly 1A1A15 at L4-1, L4-3, L3-1, and L3-3. The output 115-vac, 400-Hz, 3-phase power from E4, E6, and E8 of filter assembly 1A1A15 is applied through CB2 to standby relay 1A1K1-A2, B2, and C2 and to phase sensing relay 1A1K5PH A, PH B, and PH C. Phase sensing relay K5 monitors the phase rotation of the input ac power and operates to provide a path from 1A1K5-A2 to 1A1K5-A1 for the +5-vdc power supply to be monitored by power control 1A1A6. A missing or improper phase rotation causes K5 to open and remove the +5 vdc from power control 1A1A6 14.

(2) Setting the power mode switch 1A1S1 to STBY causes standby relay 1A1K1 to operate applying phase A through contacts A1 and A2; phase B through contacts B1 and B2; and phase C through contacts C1 and C2; to the power transformer 1A1T1, pins 1, 2, and 3 respectively. This power is also applied to the open contacts of operate relay 1A1K2-A2, B2, and C2. The secondary of 1A1T1 develops 20.9-vac, 400Hz, 3-phase power for the -15-vdc and +15-vdc power supplies 1A1A1 and 2A1A14, respectively; 232-vac, 400-Hz, 3-phase power for the 250/150vdc power supply 1A1A3; 10.4-vac, 400-Hz, 3phase power for the integrated circuit (+5 vdc) power supply 1A1A2; and 10.8-vac, 400-Hz, 3phase power for the storage/tube filament (6.3 vdc) power supply 1A1A5. The same 115-vac, 400-Hz, 3-phase power applied to power transformer 1A1T1 is also applied to 1A1J3-C, D, and E to apply to converter test set, unit 2. The 115 vac, 400 Hz, phase A is applied to ELAPSED TIME meter 1A1M1.

(3) Setting the power mode switch 1A1S1 to OPR causes the operate relay 1A1K2 to operate and apply 115-vac, 400-Hz, phase-A power through Al and 2; phase B through B1 and B2; and phase C through C1 and C2; to 1A1J5J, K, and L to apply to the unit under test.

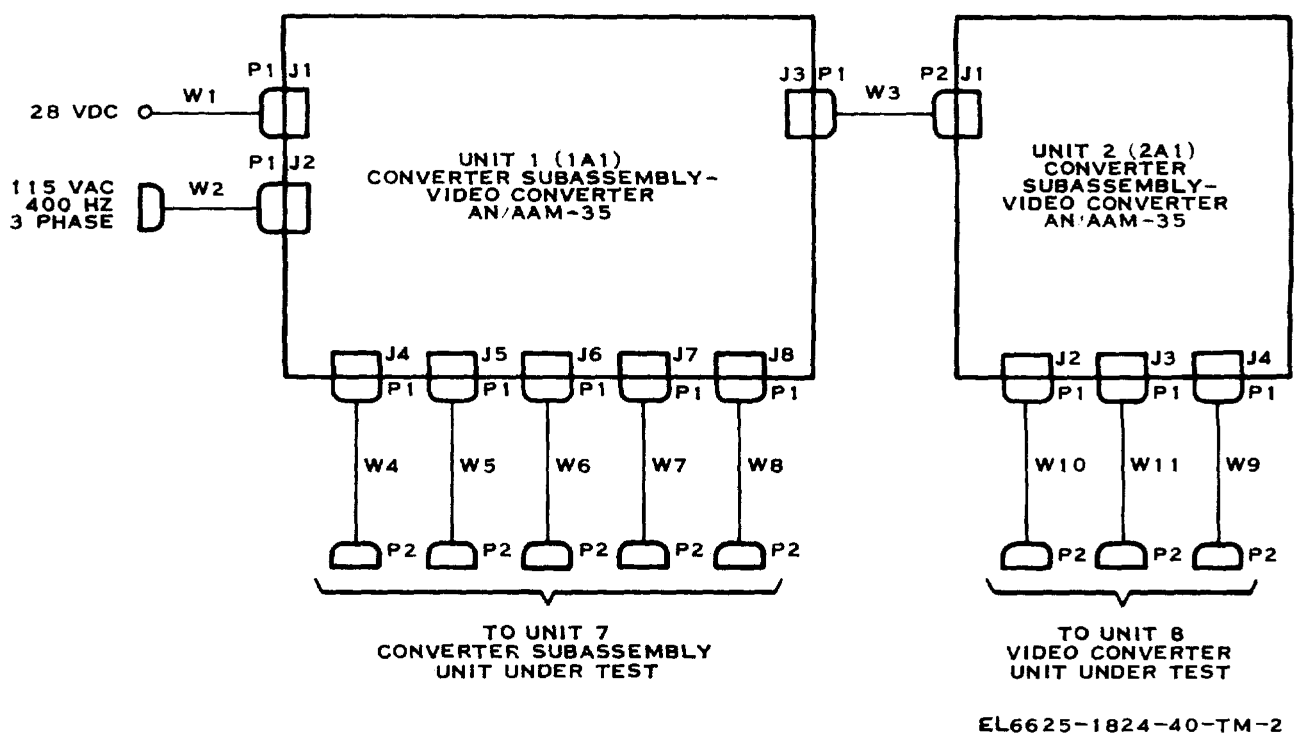


Figure 2-1. Interconnecting diagram.

b. Dc Power Distribution.

(1) The 28-vdc power enters the converter test set through 1A1J1-A and B and is applied to filter assembly 1A1A15-L2-1 and L2-3. The output from the filter assembly is at 1A1A15-E2 with a 28-vdc return established at 1A1A15-E3. The 28-vdc output is applied through diode CR1 to standby relay contact 1A1K1-D2 and to power mode switch wipers 1A1S1A-C1 and 1A1S1B-C1.

(2) Setting the power mode switch 1A1S1 to STBY applies 28 vdc through 1A1S1A-2 to standby relay 1A1K1-X1 causing it to operate and connect 28 vdc through closed contacts D1 and D2 to 1A1S1A-C2 and through operate relay 1A1K2-D2 and D3 restored contacts to light the STBY lamp DS2.

(3) Setting the power mode switch 1A1S1 to OPR continues the same operation as in (2) as 1A1S1A-2, 3, and 4 are connected together, and in addition applies 28 vdc through 1A1S1AC2 to 1A1S1A-7 to operate relay 1A1K2-X1 causing it to operate. When 1A1K2-D2 and D3 contacts open, the STBY lamp DS2 extinguishes and the 1A1K2-D1 and D2 contacts close to apply 28 vdc through 1A1J5-A to the unit under test; to DS3-2 to light the OPR lamp; and to power relays 1AlK3-X1 and 1A1K4-X1, causing them to operate. When power relays 1A1K3 and 1A1K4 operate, the closed contacts cause power to be distributed as in table 2-1 through 2-7.

Table 2-1. -15 Vdc Distribution

From	*To*
1A1A1A-6	1A1A6-20
1A1A6-20 through 1A1K3-B1 and B2	1A1A9-1
	1A1A8-22
	1A1A10-22
	1A1S3A-C1 and 02
	1A1J3-M
1A1J3-M through cable W3	2A1J1-M
2A1J1-M	2A1A12-21
	2A1A6-22
	2A1A13-10
	2A1S4-8
	2A1A1-18
	2A1A3-2
	2A1A4-22
	2A1A7-22
	2A1A5-22
	2A1A8-22
	2A1A10-22
	2A1A9-22
	2A1A11-22
	2A1S6A-C1 and C2
	2A1S11-6

Table 2-1. -15 Vdc Distribution-Continued

From	*To*
	2A1R2-2
	2A1R1-2
	2A1J3-Z, W, f and c
	2A1K3-A2
2A1K3-A2 and A1	2A1J3-DD

Table 2-2. +5 Vdc Distribution

From	*To*
1A1A2-1	1A1R17
	1A1K5-A2
1A1K5-A1	1A1A6-14
1A1A6-14 through	1A1A9-9
1A1K3-A1 and A2	1A1A7-22
	1A1A10-31
	1A1J7-F
	1A1J3-N
	2A1J1-N
1A1J3-N through cable W3	2A1A8-21
2A1J1-N	2A1A2--21
	2A1S4-6
	2A1K2-C1 and C2
2A1K2-C1 and C2	2A1J3-CC

Table 2-3. +250 Vdc Distribution,

From	*To*
1A1S3-16	1A1A6-5
	1A1K4-B2
1A1K4-B1 and B12	1A1J3-R
1AJ3-R, through cable W3	2A1J1-R
2A1J1-R	2A1S4-4
	2A1K3-C2
2A1K3-C1 and C2	2A1J3-GG

Table 2-4. +150 Vdc Distribution

From	*To*
1A1A4-16	CR7
CR7	1A1A-18
1A1K4-A1 and A2	1A1K4-A2
1A1J3-P through cable W3	1A1J3-P
2A1J1-P	2A1J1-P
	2A1A15-9
	2A1R23-1
	2A1A12-16
	2A1S4-5
2A1J1-P	2A1K3-B2
2A1K3-B1 and B2	2A1J3-FF

Table 2-5. +6.3 Vdc Distribution

From	*To*
1A1A13-23	1A1K3-C2
1A1K3-C1 and C2	1A1J3-
1A1J3-J through cable W3	2A1J1-J
2AJ1-J through 2A1K2-A1 and A2	2A1LJ3-K

Table 2-6. +6.3 Vdc Return Distribution

From	*To*
1A1A13-25	1A1K3-D2
1A1K3-D1 and D2	1A1J3-K
1A1J3-K through cable W3	2A1J1-K
2A1J1-K through 2A1K2-B1 and B2	2A1J3-L

Table 2-7. +15 Vdc Distribution

From	*To*
2A1A15-4	2A1J1-t
2A1J1-t	1A1A6-1, 16
	1A1K4-CR
1A1K4-C1 and C2	1A1A9-23
	1A1A8-23
	1A1S6-6
	1A1J3-L
1A1J3-L through cable W3	2A1J1-L
2A1J1-L through 2A1K2-D1 and D2	2A1J3-EE

Table 2-7. +15 Vdc Distribution--Continued

From	*To*
2A1J1-L	2A1A12-8
	2A1A6-23
	2A1A13, 17
	2A1S4-7
	2A1A1-22
	2A1A2-23
	2A1A3-23
	2A1A4-23
	2A1A7-23
	2A1A5-23
	2A1A8-23
	2A1A10-23
	2A1A9-23
	2A1A11-23
	2A1S5-1
	2A1S11-3
	2A1J3-g, a, d, X

Section III. PRINTED CIRCUIT BOARD AND INTEGRATED CIRCUITS FUNCTIONING

2-5. Converter Test Set and Detecting Set Common Boards

Some printed circuit boards in the converter test set are identical to printed circuit boards in Detecting Set, Infrared AN/AAS-24 (detecting set). For a general description of these boards, refer to TM 11-5850-241-50. These boards are listed in table 2-8. The converter test set board reference is listed in the converter test set column and the detecting set reference designator is listed in the detecting set column.

Table 2-8. Cross Reference of Converter Test Set Printed Circuit Boards to Detecting Set Printed Circuit Boards

Converter test set	Detecting set
1A1A1	7A4
1A1A2	7A5
1A1A5	7A6
1A1A8	7A19
2A1A2	7A23
2A1A3	7A21
2A1A4	7A9
2A1A5	7A8
2A1A6	7A17
2A1A7	7A12
2A1A8	7A11
2A1A9	7A10
2A1A10	7A16
2A1A11	7A15
2A1A14	7A3

2-6. 250/150-Vdc Power Supply, 1A1A3
(fig. 2-2)

The 250/150-vdc power supply provides 250 regulated volts dc. The circuit has built-in overload protection and automatic reset capability.

a. The 232-vac, 400-Hz, 3-phase power is applied to 1A1XA3-2, 4, and 8, rectified by diodes CR1 through CR6 to provide unregulated voltage at P1-10 which is applied to heatsink assembly 1A1A14-1. Regulation is provided by two Darlington pairs of series regulators, 1A1A3Q8 and Q9 and 1A1A14Q1 and Q3. Control of these series regulators is provided by comparator 1A1Z1, preregulator 1A1Q1 and potentiometer 1A1R20. Any voltage fluctuation across 1A1R20, which is sensitive to changes at the output pin 16, is applied to 1A1Z1-3 (noninverting input). The output at 1A1Z1-6 determines conduction of 1A1Q1 which biases the series regulating transistors 1A1Q8 and 1A1Q9. This action also adjusts the conduction of the two external series regulating transistors in heatsink 1A1A14.

b. Overload protection is provided by the foldback circuit composed of actuator 1A1Q4, sustainer 1A1Q6 and diode 1A1CR15 (foldback is defined as a current limit automatically reducing to a lower current when an overload occurs in order to limit power dissipation in the series elements). When an overload occurs, 1A1Q4 conducts and biases 1A1Q6 into conduction. The 1A1Q6 collector is connected to the base of 1A1Q4 and a latch-up occurs. The negative going signal at the collector of 1A1Q4 is applied through CR15 to decrease conduction in the series regulators, thereby decreasing load current. This decrease is the overload protection for the 250vdc power supply and the load circuitry.

c. An initial foldback inhibit circuit composed of 1A1Q5 and Q7 prevents latch-up of the foldback circuit when activating the converter test set. A false indication of overload could cause latch-up as by-pass or load capacitors charge, so the foldback inhibit prevents latch-up upon initiation of power for approximately one second. The initial power application starts 1A1C12 charging and causing 1A1Q7 to conduct. The emitter of 1A1Q7 attached to the base of 1A1Q5 causes conduction and a negative going signal applied to the base of 1A1Q4 prevents conduction and foldback during A1C12 charge. The long time constant charge holds this state for approximately one second and then reverts to normal condition.

d. The auto-reset oscillator composed of 1A1Q1, Q2, Q3, CR9, and C8 pulses 1A1Q6 at approximately one-second intervals with a negative going pulse to cut 1A1Q6 off, which in turn cuts 1A1Q4 off. If the overload is still present, the latch-up is repeated. If the overload is not present, the power is reapplied to the load. The oscillator does not normally function, but when the foldback circuit is activated, the voltage developed across CR7 powers it for operation.

2-7. 250/150-Vdc Power Supply, 1A1A4

(fig. 2-2)

The 250/150-vdc power supply 1A1A4 generates 150 vdc for use in the converter test set and for the unit under test. Operation and analysis are identical to 250/150-vdc power supply 1A1A3 with the exception of the input. The input to pin 2 is the 250-vdc unregulated voltage from 250/ 150-vdc power supply 1A1A3. This input is applied through CR1 to P1-10 and analysis of the circuit from this point on is the same as 1A1A3. The external resistors set the operating point and 1A1A4R20 determines the input to 1A1A4Z1 for +150-vdc operation instead of + 250 vdc.

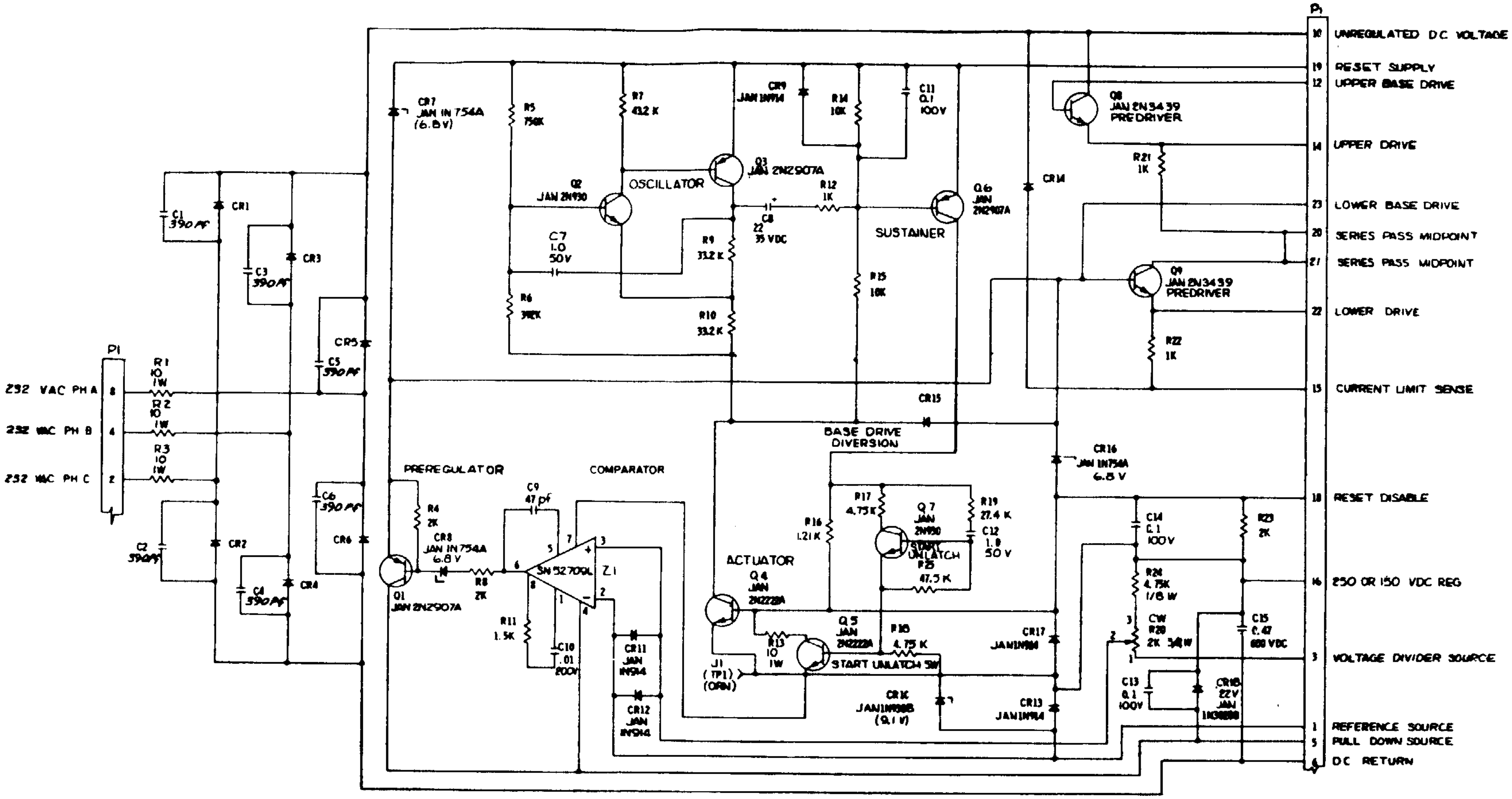
2-8. Power Control, 1Al1A6

(fig. 2-3)

The outputs of the +250-vdc, +150-vdc, +15-vdc, + 5-vdc, and -15-vdc regulated power supplies are applied to 1A1A6P1-5, P1-18, P1-16, P1-14, and P1-17 as sense voltages. If any of the five voltages sensed by the power control circuit exceeds the overvoltage or undervoltage limits, the dc return to operate relay 1A1K2 is removed, causing it to restore and remove the 28 vdc to power relays 1A1K3 and K4, removing power from unit 2 and the unit under test. The five sense voltages are applied to five voltage dividers, consisting of R4 through R11 and R27 and 29, which reduce each of the applied voltages to three volts. The divided voltage from the -15-vdc power supply is inverted by unity-gain amplifier Z1. The five +3-vdc levels are applied through R12, R13, R14, R20 and R28 to the level detectors as an OR function and deviations in any one of the sensed voltages will appear at C4. The OR function is applied to noninverting input Z2-3 and to inverting input Z3-2. A reference voltage is developed by resistor R1 and zener diodes CR1 and CR2. The reference level for overvoltage detector Z2 is established by potentiometer R21; the reference level for undervoltage detector Z2 is established by potentiometer R21; the reference level for undervoltage detector Z3 is established by R19. If the OR function input is either higher than the overvoltage reference level or lower than the undervoltage reference level, the output at Z2-6 or Z3-6 is high, biasing transistor Q1 on, increasing the voltage drop across R26, and biasing transistor Q2 off. When transistor Q2 is cut off, relay 1A1A6K1 is open and the 28-vdc return circuit is opened. FAIL power of 28 vdc is applied from 1A1A6-4 through relay 1A1A6K1-B2 and B3 to relay 1A1A6K2-X1 causing it to operate and apply 28 vdc through 1A1A6-7 to light FAIL lamp 1A1DS1. Latch-out power of 28 vdc enters at 1A1A6-9 and is applied through 1A1A6K2A2 and A1 to latch 1A1A6K2 in the operate condition and maintain the FAIL lamp signal even if proper operating power returns. It is necessary to set the power mode switch to RESET or STBY to remove the latch-out power furnished by power mode switch 1A1S1B-3 to 1A1A6-9. This action allows 1A1A6K2 to restore and 1A1A6K1 to operate before reapplying latch-out power to 1A1A6-9. Resistors R22, R23, and R24 provide failsafe protection against the failure of amplifiers Z2 and Z3.

NOTE

Power control 1A1A6 can light the FAIL lamp in either standby or operate mode. Power cannot be applied to the external jacks in unit 2 unless the safety interlock is completed. Connections to the unit under test completes this circuit. The connection may be simulated by connecting a jumper between 2A1J3-H and J.



NOTES: UNLESS OTHERWISE SPECIFIED

1. DIODES ARE JANIN3613.
2. RESISTORS ARE 1/4 WATT.
3. CAPACITORS ARE 500 VOLTS.
4. RESISTANCE VALUES ARE IN OHMS.
5. CAPACITANCE VALUES ARE IN MICROFARADS.
6. REFERENCE DESIGNATION PREFIX 1A1A8, 1A1A3, OR 1A1A4.

EL6625-1824-40-TM-3

Figure 2-2. 150/250-vdc power supply 1A1A3 and 1A1A4, schematic diagram.

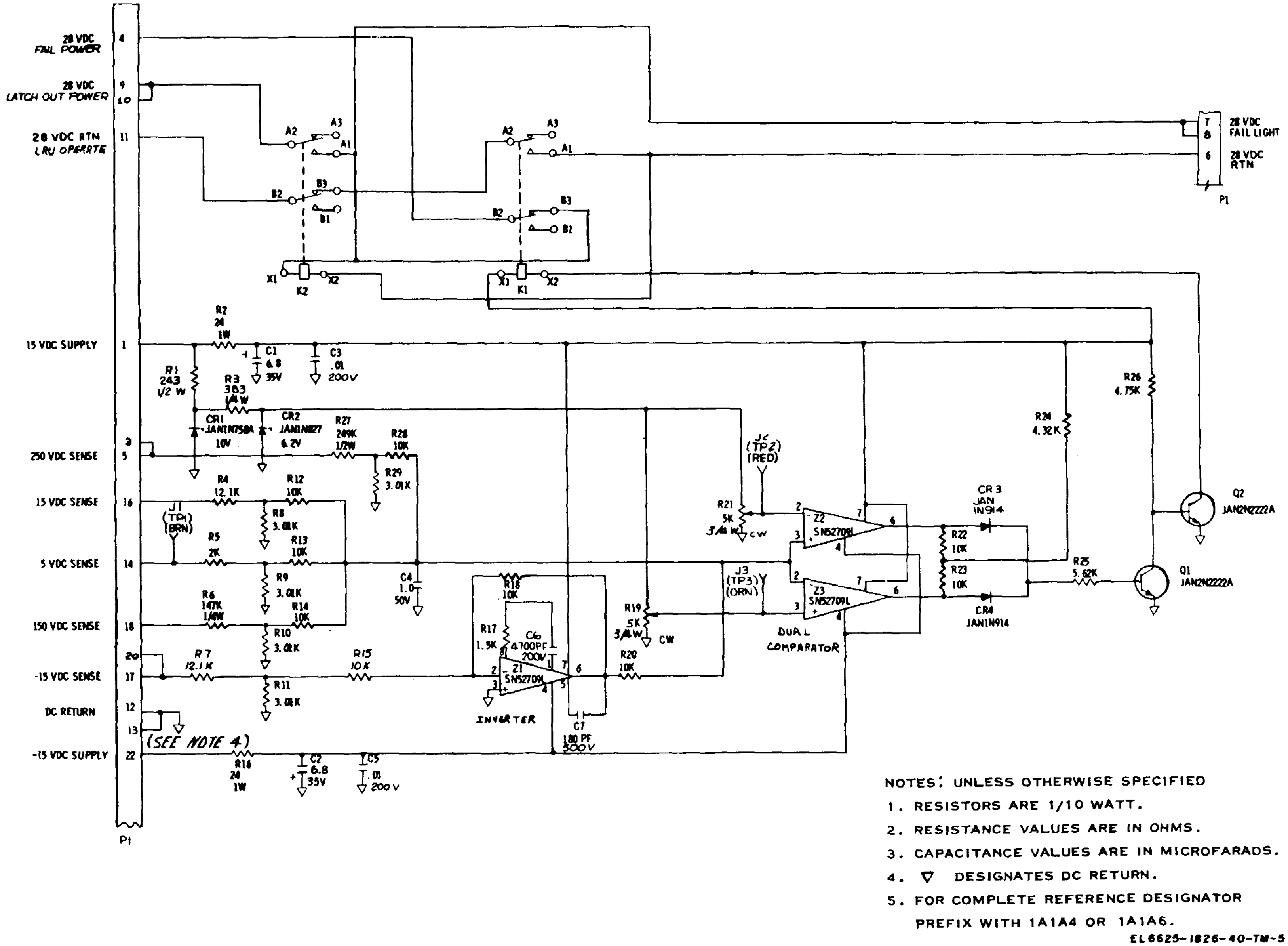


Figure 2-3. Power control 1A1A6, schematic diagram.

2-9. Cs-Vc Simulator, 1A1A7

(fig. 2-4)

The simulator provides video gate, video gate, and simulated video output signals in response to 100 kHz input signals. Video gate and video gate are square wave signal voltages obtained by dividing the 100 kHz signal by 504. The simulated. video signal is obtained by using the video gate signal 'to gate an oscillator, which in turn operates at the simulated video frequency.

a. The 100 kHz input signal is applied to connector P1-4 from unit 2 of the converter test set. Connector P1-4 is connected internally to a divide-by-seven circuit consisting of NAND gate Z1, and flip-flops Z2 and one half of Z3. At the end of the 7-count, flip-flop Z2 is reset by applying logic 1 to NAND gate Z1B inputs from Z2-12, Z2-9, and Z3-12. The output signal from the divide-by-seven circuit applied to the divide-by-eight circuit at Z3-5 is 14.285 kHz. The divide-by-eight circuit divides the frequency to 1.785 kHz and applies the signal to the input of the divide-by-nine circuit at Z5-14.

b. The divide-by-nine circuit consists of flipflops Z5, Z7, and NAND gate Z6C and D. At the end of the 9-count, Z5 input flip-flop is reset by applying logic 1 to Z5-14 from Z7-8. This 9-count feedback is accomplished in the following sequences. At the end of the 8-count, a logic 1 is applied to the three inputs of Z6C from Z5-12, Z5-9, and Z7-12. This produces a logic 1 at Z7-7. The next count at the input of the divide-by-nine circuit is also applied to Z7-5. This produces a 1 logic 1 at Z7-8 that is fed back to Z5-14, resetting the circuit. Resetting the circuit starts the logic 0 output at Z7-12 that is applied to connector P1-8 and the input of Z6E. The output switches to a logic 1 at the beginning of the next 9-count. The output frequency at connector P1-23 and 8 is reduced to 198.4 Hz. A frequency of 198.4 Hz is equivalent to gate pulses 5040 microseconds in duration.

c. The video gate signal is applied to the base circuit of inverter amplifier Q1. The signal is amplified by Q1 and Q4 providing a switch for oscillator Q3. The oscillator is gated on when transistor Q2 is not conducting. The oscillator frequency is a function of the RC time of capacitor C3 and resistor R4. Adjusting the potentiometer changes C3 voltage and the frequency. The oscillator output signal is inverted at the collector of transistor Q5 and used to trigger the monostable multivibrator. The multivibrator, consisting of transistors Q6 and Q7, shapes the pulses and applies the signal to emitter-follower Q8. The emitter-follower signal output is adjusted by video level adjust potentiometer R17. The potentiometer output is then applied to connector P11.

2-10. Sync Interface, 1A1A9

(fig. 2-5)

Sync interface circuits provide interface between sync signals generated by circuits in unit 1 of the converter test set, to the unit under test.

a. Simulate video signals are applied to connector PI-10 from simulator 1A1A7. The signals are applied to buffer Z5. Buffer Z5 provides three identical video gate output signals. The signals from Z5A, C and D are applied to COUNTER switch S11-1, to unit 2 of the test set and the unit under test, and to hotspot and slew voltage generator 1A1A1.

b. The input to dc amplifier Z6 is held to approximately -0.07 volts dc by resistors R22, R24, R26, and R27. Amplifier gain is determined by the ratio of feedback resistance to input resistance

$$\left(AV = 1 + \frac{\text{feedback resistance}}{\text{input resistance}} = \frac{R32}{\text{R30, R31, and R35}}\right).$$

The amplifier gain is controlled by FIELD OF VIEW switch 1A1S3. On switch positions 1/4, 1/2, and FULL, the amplifier gain is 12, 6, and 3, respectively. Setting the switch to 1/4 applies -15 volts dc to connector P1-18 and ground potential to P1-21. Transistor Q3 is saturated, applying ground potential to the junction of resistors R30 and R31. Transistor Q4 is cut off. Amplifier gain is determined by the ratio of resistor R32 to R30. Setting FIELD OF VIEW switch 1A1S3 to 1/2 applies -15 volts dc to connector P1-21 and ground potential to P1-18. Transistor Q4 is saturated, applying ground potential to the junction of resistors R31 and R35. Transistors Q3 is cut off. Amplifier gain is determined by the ratio of resistor R32 to R30 and R31. Setting FIELD OF VIEW switch 1A1S3 to FULL applies -15 volts dc to connector P1-18 and P121. Transistors Q3 and Q4 are cut off. Amplifier gain is determined by the ratio of resistor R32 to R30, R31, and R35. The amplifier output is v/h modified by the field of view function and is either -2.0, -4.0, or -8.0 volts dc for full, 1/2 or 1/4 fov, respectively.

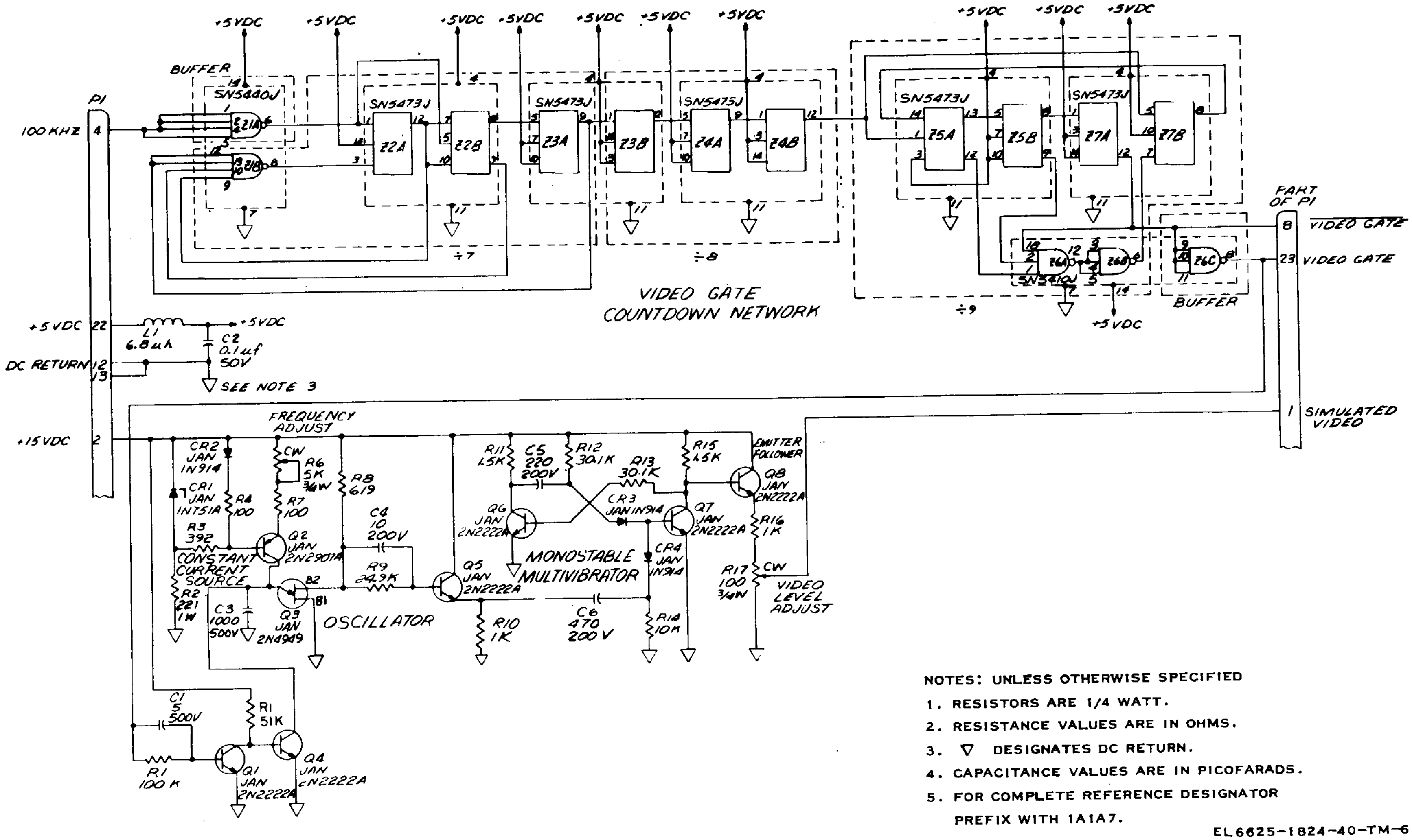


Figure 2-4. Cs-Vc simulator 1A1A7, schematic diagram.

c. Hot target and hot target signals are applied to comparator Z3 from hot target and slew voltage generator 1A1A10. Comparator Z3 output signal is a square wave. The square wave is amplified by transistor Q1 and then applied through connector P1-6 to the unit under test.

d. Resistors 1A1A9R1 and R2 form a voltage divider to provide -.05 vdc v/n test output at 1A1A9P1Z.

2-1 1. Hot Target and Slew Voltage Generator, 1A1A10

(fig. 2-6)

Hot target and slew voltage generator circuits provide hot target and hot target signals to the unit under test in response to video gate signals from the sync interface circuit. The hot target and slew voltage generator also provides selected slew voltages to the unit under test in response to a reference voltage from the unit under test.

a. The video gate signal is applied to the base circuit of inverting amplifier Q1. The signal is inverted and amplified providing a switch for oscillator Q3. The oscillator is gated on when transistor Q2 is not conducting. The oscillator oscillates at approximately 9.8 kHz. The oscillator frequency is determined I)y the charge of capacitor C3. The output voltage across resistor R9 triggers monostable multivibrator Q4 and Q5. The multivibrator shapes the pulses and applies the output pulses to inverter buffer NAND gate Z1. NAND gate Z1A inverts the input signal and applies the output to the unit under test and to the input of NAND gate Z1B. NAND gate Z1B inverts the input signal and applies the output signal to the unit under test. The signal output at connector P1-8 and 6 simulates hot target and hot target signals, respectively to the unit under test.

b. A reference voltage from the unit under test is applied to connector P1-15 and from P115 to the voltage divider resistors R7, R10, R12, R13, R15, R18 and R19. The output voltages from the divider are selected by SLEW switch S5 and applied to the unit under test. Each voltage selected represents slew angles of left 30 degrees, left 20 degrees, left 10 degrees, zero degrees, right 10 degrees, right 20 degrees or right 30 degrees.

2-12. Load Board Number One 1A1A11, and Number Two 1A1A12

(fig. 2-7 and 2-8)

The load boards provide resistors for the output circuits of the unit under test for loading or impedance matching to the circuitry of the converter test set. The load boards adjust the output of the unit under test to correspond to the signal levels of the unit under test circuit when used in the Detecting Set, Infrared AN/AAS-24. Isolation resistors prevent damage to the unit under test circuit if shorting of the output occurs.

2-13. Heatsink Assembly, 1A1A13

(fig. 2-9)

The -15 and +6.3 volts dc output assembly operates in conjunction with the associated dc power supply to supply regulated dc voltages to the respective loads. Each regulator uses a power transistor with the emitter-collector circuit connected in series with the load. A change in load is sensed at the emitter circuit of the transistor. The sense voltage is applied to amplifier and control circuits in the respective dc power supply, which in turn supplies drive to the regulator circuit. In the -15 volt dc regulator circuit, the drive is applied to a driver whose output controls the conduction of the series regulator. In the +6.3 volt dc regulator circuit, the drive is applied directly to the base of the regulator transistor. The drive voltage causes the regulator emitter voltage to oppose the change in the output voltage.

2-14. Heatsink Assembly, 1A1A14

(fig. 2-10)

The 250- and 150-vdc output heatsink operates in conjunction with the associated dc power supply to supply regulated dc voltages to the respective loads. The two power transistors 1A1A14 Q1 and Q2 provide series limiting of the regulated output current. Deviations in the output are sensed in the 1A1A14Q2 emitter circuit and applied to the amplifier and control circuits in 250/150-vdc supply 1A1A3. As in the 1A1A3 circuit description (para 2-7), drive voltages are applied to 1A1A14Q1 and Q2 bases to adjust the output current. The 1A1A4 150-vdc portion operates identically.

2-15. Filter Assembly, 1A1A15

(fig. 2-11)

Filter assembly 1A1A15 protects the converter test set internal components from induced or power source generated transients. The 115-vac, 400-Hz, 3-phase power is applied through suppressor coils 1A1A15L3 and L3, across 1A1A15R1, R2, R3, and R4 and through 1A1A15FL1 through FL4. The filtered output is

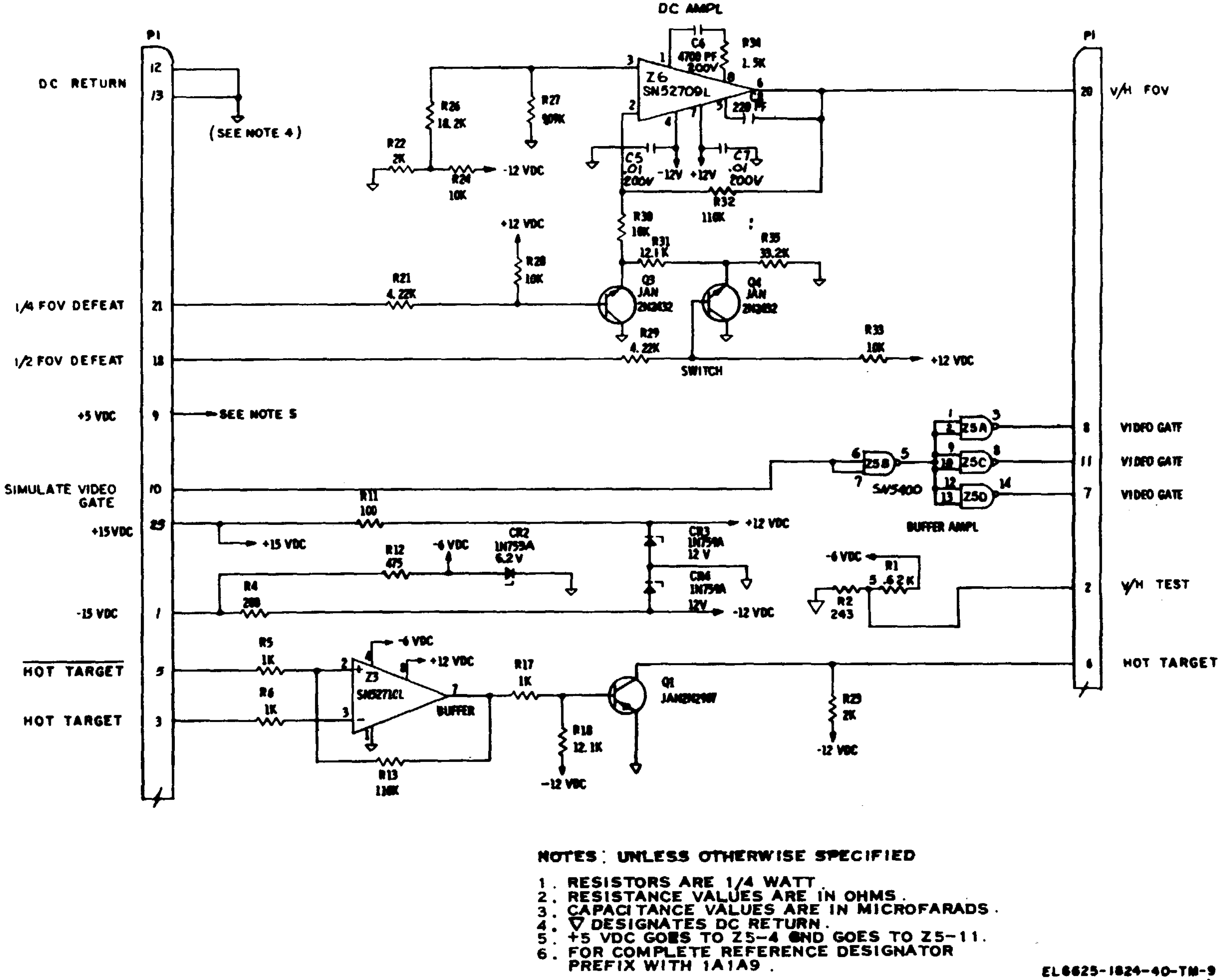


Figure 2-5. Sync Interface 1A1A9, schematic diagram.

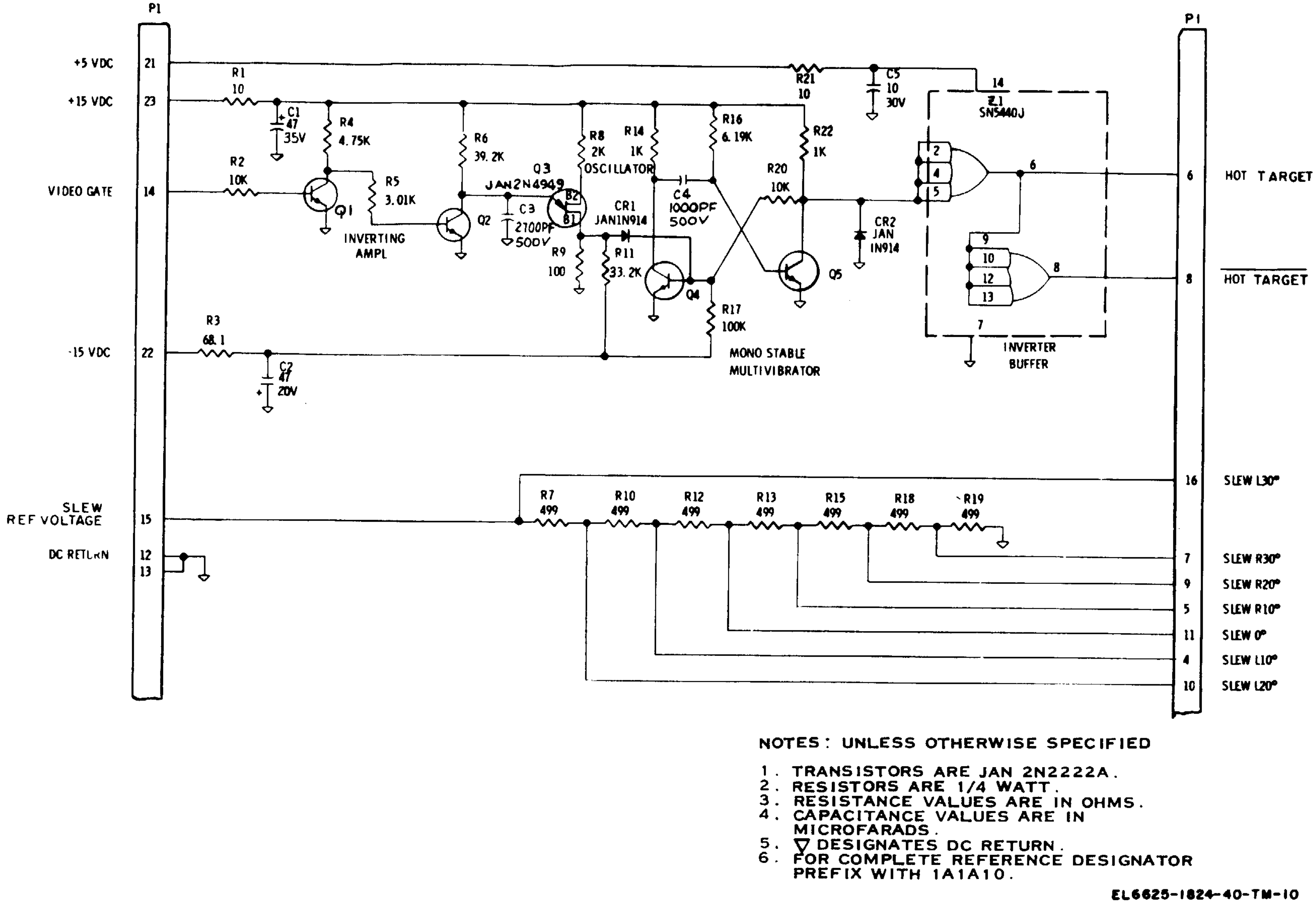


Figure 2-6. Hot target and slew voltage generator 1A1A10, schematic diagram.

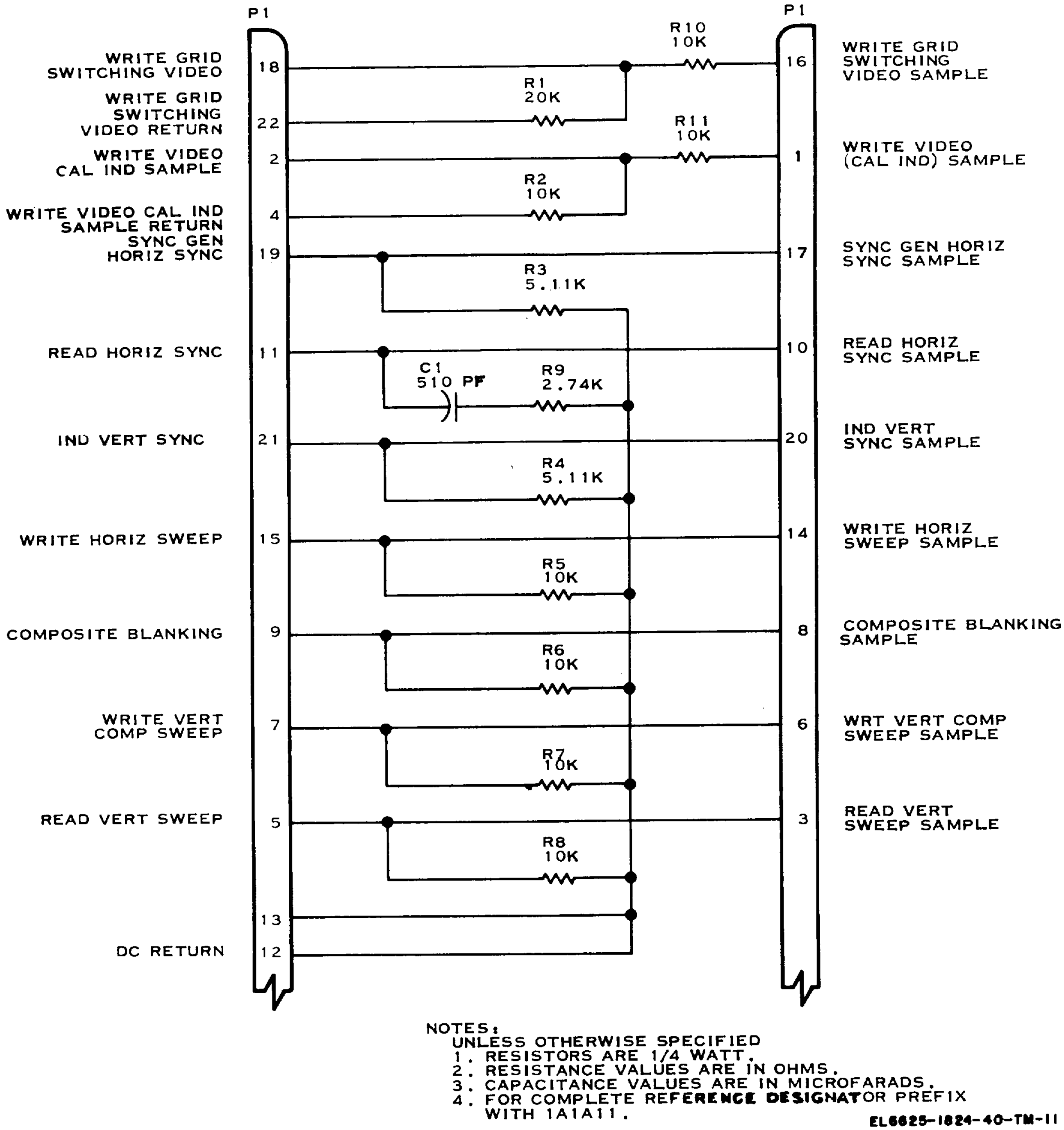


Figure 2-7. Load board number one 1A1A11, schematic diagram

applied through 1A1A15L5 and L6 and across capacitors 1A1A15C2, C3, and C4. The ac output at 1A1A15E4 is phase A; E6 is phase B; E8 is phase C; and E9 is neutral. The 28-vdc input at 1A1J1-A is applied through 1A1A15L2, FL5 and 6, L1, and across C1. The 28-vdc output is at 1A1A15E2. The return is at E3.

2-16. Signal Generator, 2A1A1
(fig. FO-6)

Signal generator 2A1A1 is divided into three sections, frame hold, 100 kHz, and gated video.

a. In quiescent state, voltage divider 2A1A1R16 and 17 develop a high input to transistor switch 2A1A1Q1

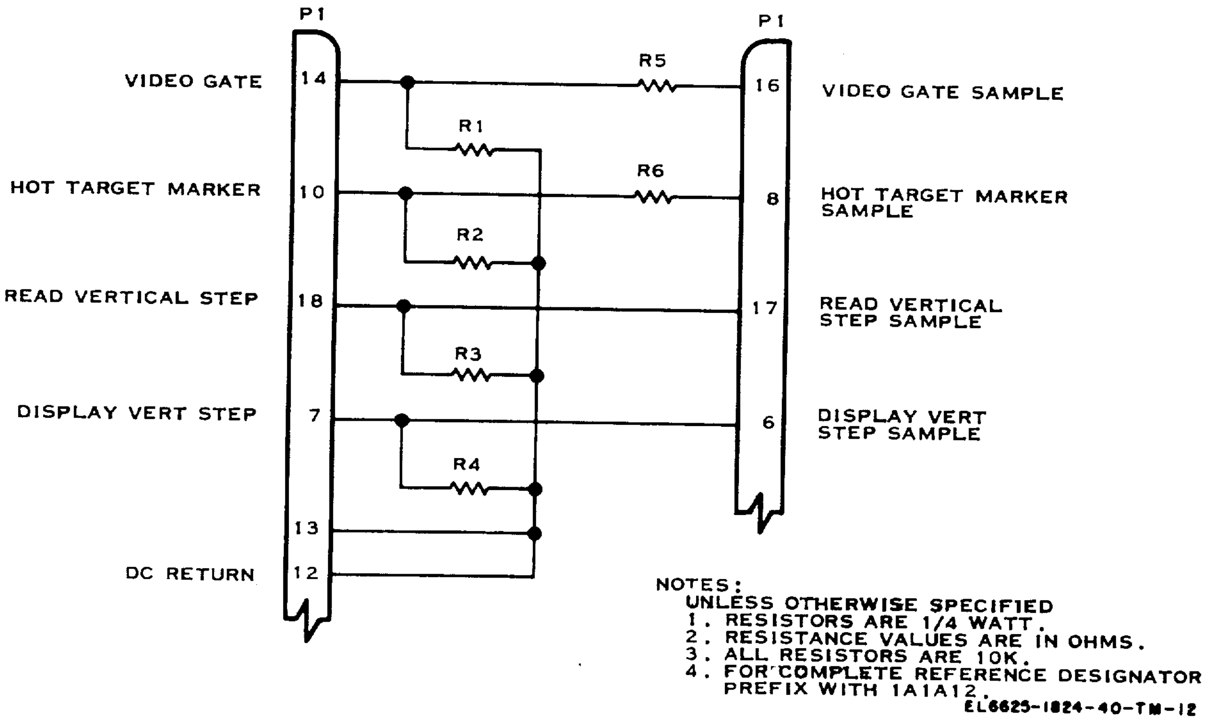


Figure 2-8. Load board number two 1A1A12, schematic diagram.

causing conduction and an effective ground signal output to 2A1J2-L. FRAME HOLD switch 2A1S5 applies a ground to 2A1A114 to the base of switch Q1, cutting it off. This applies an open to 2A1J2-L as the frame hold signal.

b. The 100 kHz oscillator is a crystal-controlled oscillator employing an operational amplifier 2A1A1Z1. Amplifier Z1 is driven to saturation and cutoff. Crystal Y1 sets the frequency at 500 kHz and provides the necessary regenerative feedback to sustain oscillation. The feedback is developed across R8 and applied to the noninverting input Z1-2. The 500-kHz output is inverted in Z3 and applied to the divide by 5 counter Z5. The 100 kHz output is applied to 2A1A1-21.

c. The 500 kHz is applied in parallel to two (divide by 3 counters in Z1. The output of the first divide by 3 counter is applied to 2A1A1Z21 along with the 500 kHz signal at Z2-2. The output is buffered by dual inversion with an input to 2A1A1Z2-13. The duty cycle at this point is approximately 25 percent. The input to Z2-12 lengthens this cycle to 50 percent. The output is gated by the video gate input at 2A1A1-3 and the switched +5 vdc at 2A1A1-2 (reference waveform AL, figure 3-2).

2-17. Sweep and Blanking, 2A1A12

(fig. 2-12)

The sweep and blanking 2A1A12 generates a horizontal and vertical sweep output for application to an external scope. In addition, the blanking pulse is generated to apply to storage tube protect, loads, and video amplifier 2A1A13.

a. The horizontal sync input to 2A1A12-14 triggers the multivibrator composed of 2A2A12Q1 and Q3. This output triggers the multivibrator composed of 2A2A12Q6 and Q8. This output is applied to amplifier 2A2A12Q9. The amplified output starts the sweep generators 2A1A12Q10 and Q12. The linear sweep output is taken from the collector of 2A2A12Q12 and applied to P1-23 and to an external test point X OSCP (reference waveform V, figure 3-2).

b. The vertical sweep circuitry is identical to the horizontal sweep circuitry except that only one multivibrator is used. The vertical sweep output is at 2A1A12-1 (reference waveform W, figure 3-2).

c. The blanking pulse is generated by the same trigger pulses which activate the sweep circuitry. The negative pulses are applied through 2A2A12CR12 and 13 to 2A2A12Q11. This output is applied to P1-5 and to the storage tube protect, loads, and video amplifier 2A1A13 (reference waveform A1, figure 3-2).

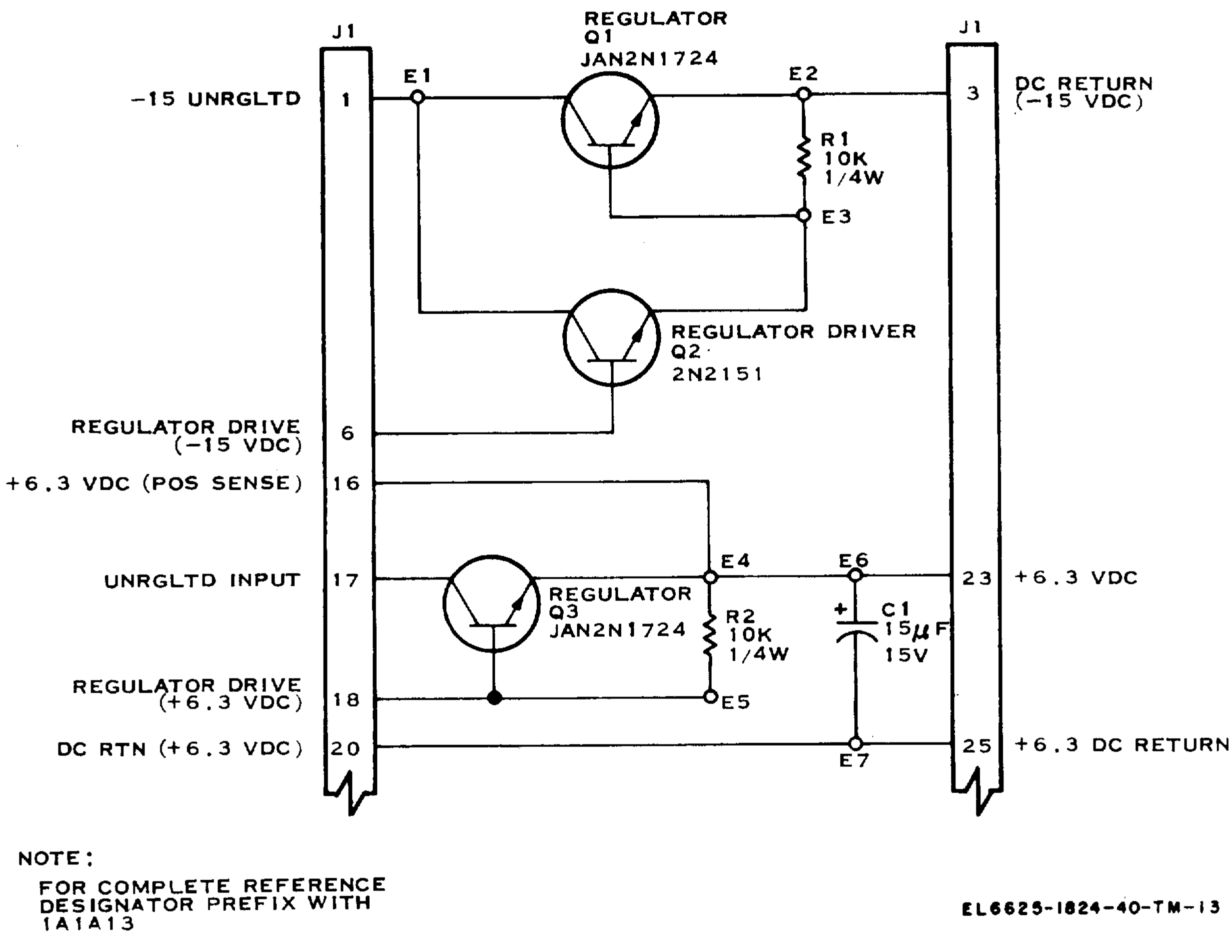


Figure 2-9. Heatsink assembly 1A1A13, schematic diagram.

d. The focus test drive output depends upon the setting of external FOCUS TEST potentiometer 2A1R23. The center tap of 2A1R23 is applied at 2A2A12-18 for application to the base of 2A1A12Q13. The output at 2A1A12-20 is applied to heatsink 2A1A15Q3 to control the 100 vdc output.

2-18. Storage Tube Protect, Loads, and Video Amplifier, 2A1A

(fig. 2-13)

The storage tube protect, loads, and video amplifier 2A1A13 has three functions: the 28-vdc protect signal output is applied to the unit under test; the read video is blanked and amplified then applied to an external test point for scope monitoring; and frame hold and field of view signals from the unit under test are loaded and applied to external test point LRU C for analysis.

a. The storage tube protect bite signal is applied through 2A1A13-18 to 2A1A13Q6. This positive going signal turns Q6 on and the resulting positive potential on the emitter turns Q7 on to operate 2A1A13K1. The 28 vdc at 2A1A13-20 is applied through the closed contacts of 2A1A13-K1 to 2A1A13-22 and out to the unit under test.

b. The read video from the unit under test is applied to 2A1A13-11. The blanking signals from sweep and blanking 2A2A12 are applied to 2A1A13-5. Both signals are applied to the base of 2A1A13Q1. While the blanking signals are applied, Q1 is saturated. The read video signal passes between the blanking signals to 2A1A13Q3. Transistor 2A1A13Q3 drives the push-pull amplifier composed of 2A1A13Q4 and Q5. Degenerative feedback drives 2A1A13Q2 for constant gain and linearity and the output is applied from 2A1A13-9 to external test point Z OSCP for monitoring.

c. Frame hold and field of view samples from the unit under test are applied to 2A1A13-21, 19, 8, 7, and 6. Load resistors R24 through R28 load the samples. The frame hold and fov samples are then applied from 2A1A13-23, 2, 1, and 3 to LRU 2A1S9 for monitoring.

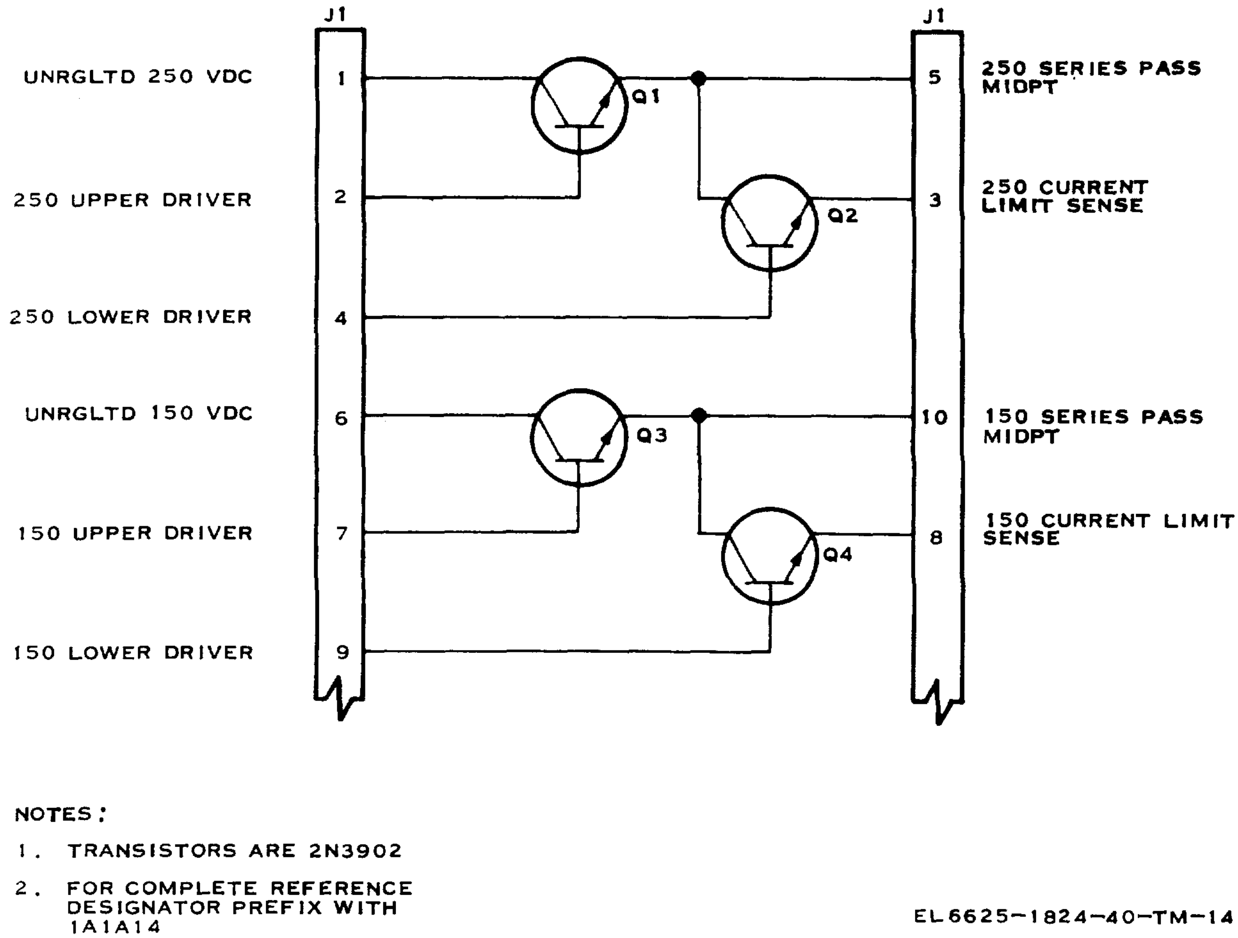


Figure 2-10. Heatsink assembly 1A1A14, schematic diagram.

2-19. Heatsink Assembly, 2A1A15
(fig. 2-14)

The +15-vdc heatsink regulator is identical to the -15-vdc portion of. heatsink assembly 1A1A13. Refer to para 2-13 for a functional ,description of this portion of heatsink assembly 2A1A15. The focus voltage regulator input is +150 vdc at 2A1A15-9. The regulating signal is applied through 2A1A15-12 to the base of 2A1A15Q3. The 100-vdc output is applied to 2A1A15-15.

2-20. Integrated Circuits

a. Integrated Digital Logic. The 54 series integrated circuits are. high speed, low power, general purpose circuits for digital applications. This series includes the basic gates, flipflop elements and complex logic and storage elements needed to perform all functions of general purpose logic systems. The digital logic circuits employed in the converter test set are SN5400J, SN5404J, SN5410J, SN5430J, SN5440J, and SN5473J. All units in the converter test set are suffixed by J to denote case style. All units except SN5404J are referenced in TM 11-5850-241-34. The SN5404 is a sextuple inverter; each inverter has a single input and output (fig. 2-15).

b. Operational Amplifiers. The operational amplifiers used in the converter test set are differential amplifiers which function as summing amplifiers, buffing amplifiers, and comparators. The inverting input is designated (-) while the noninverting input is designated (+). Signals applied to the inverting input cause an output signal of opposite polarity to the input. Signals applied to the noninverting input are reproduced with no inversion. These units are high performance, general-purpose amplifiers with high-impedance differential inputs and low-impedance outputs. The operational amplifiers employed in the converter test set are SN52702L, SN52709L, SN52710L, and SN52711L; all are referenced in TM 11-5850-241-34/1.

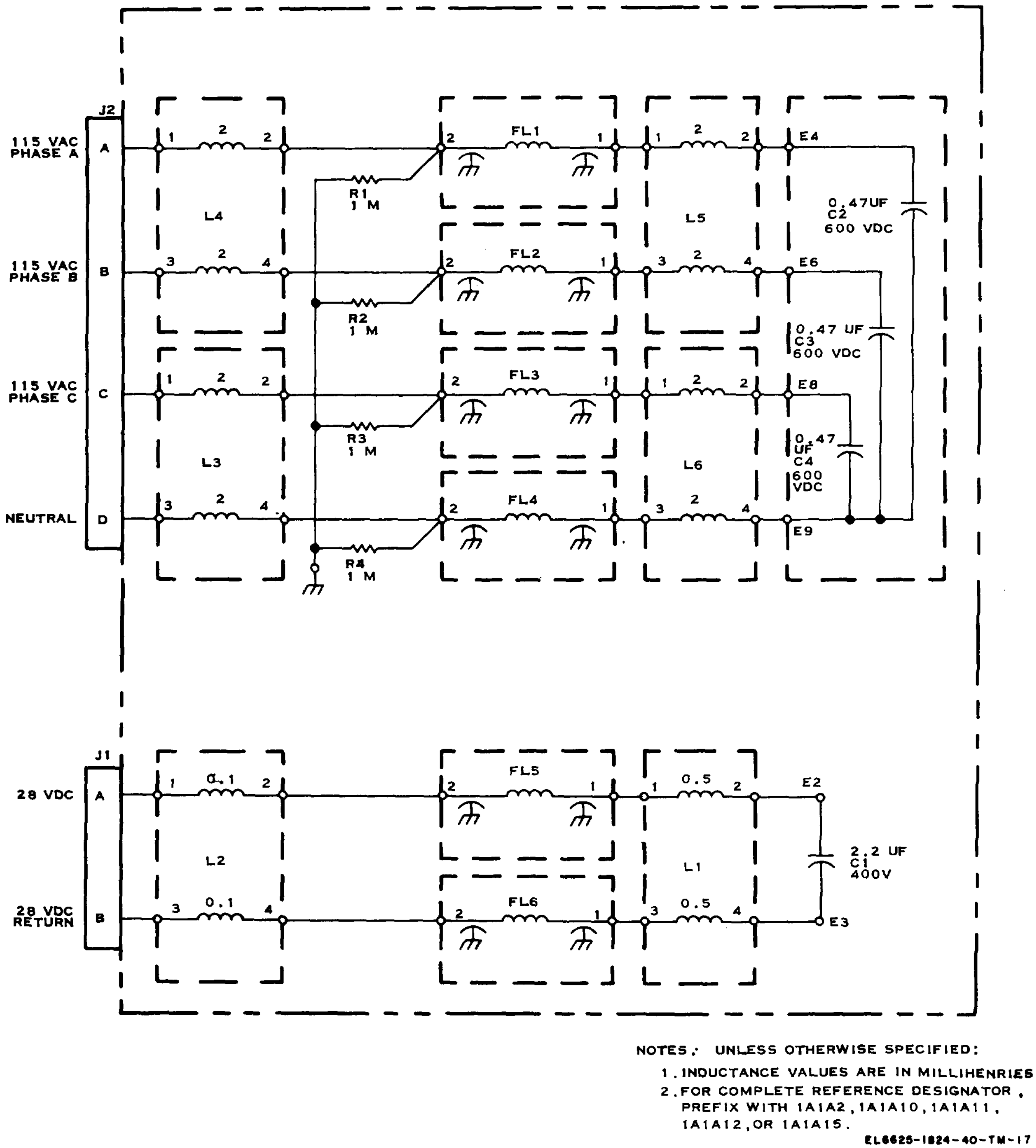


Figure 2-11. Filter assembly 1A1A15, schematic diagram.

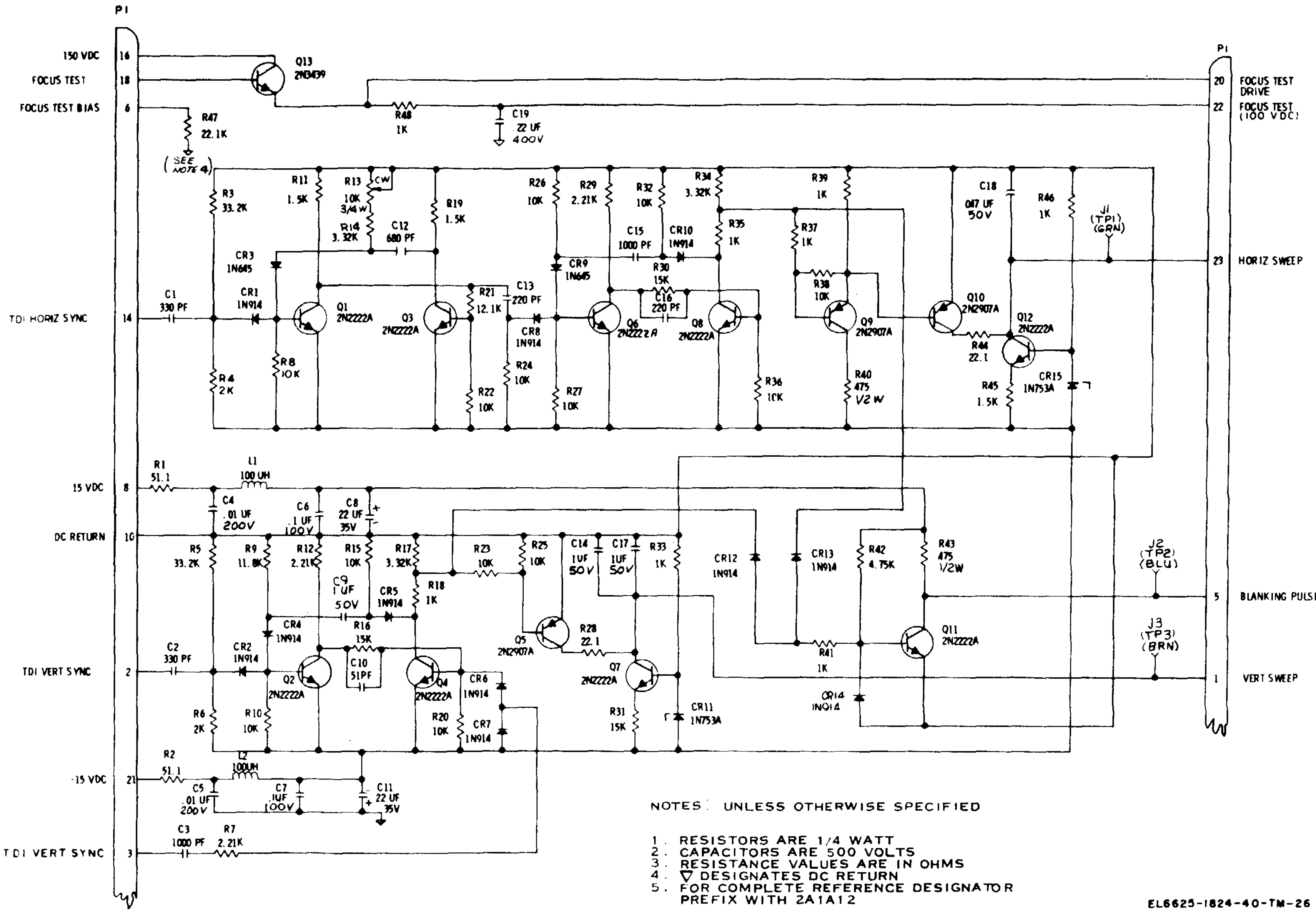
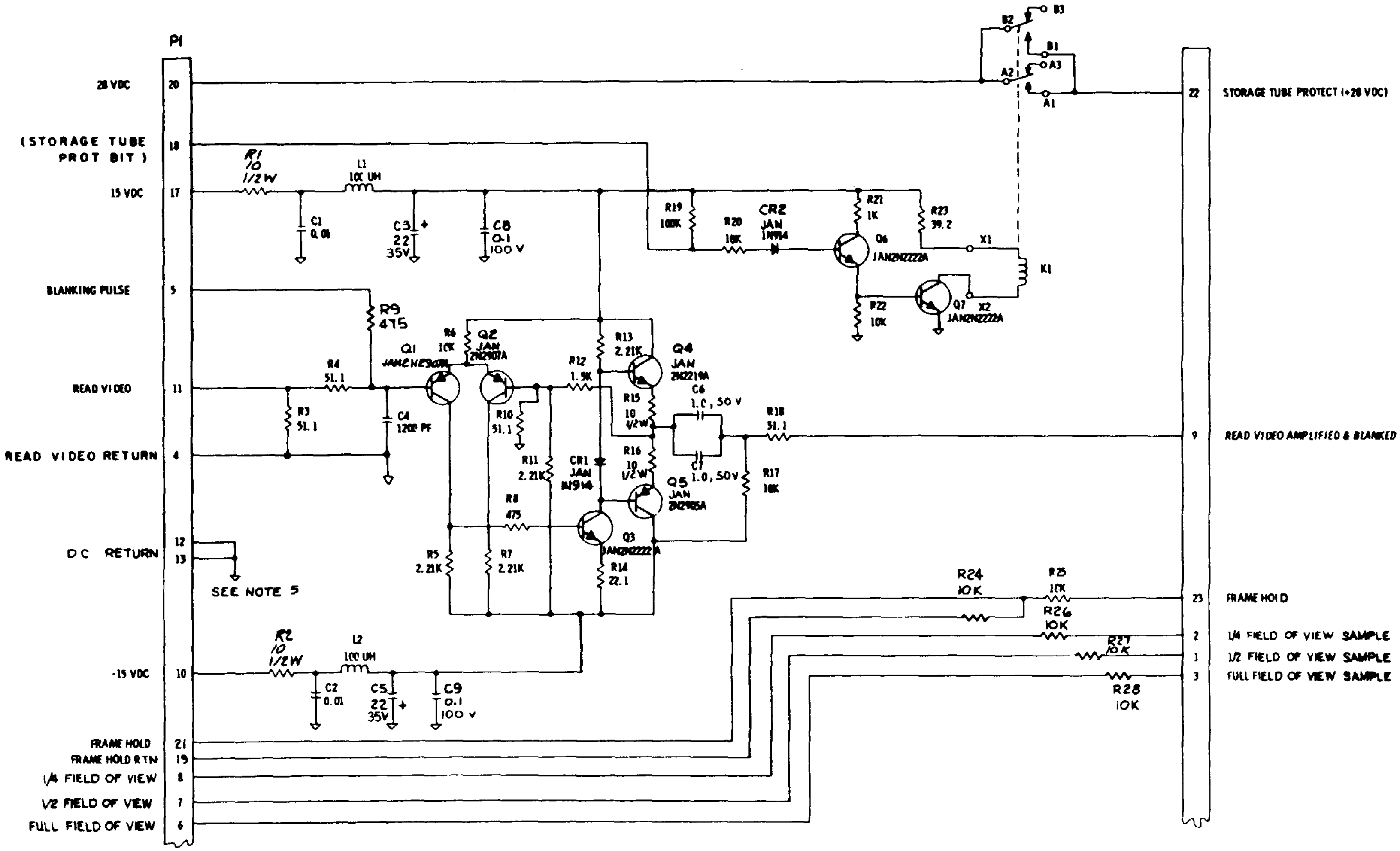


Figure 2-12. Sweep and blanking 2A1A12, schematic diagram.



NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTORS ARE 1/4 WATT
2. CAPACITORS ARE 200 VOLTS
3. RESISTANCE VALUES ARE IN OHMS
4. CAPACITANCE VALUES ARE IN MICROFARADS
5. ▽ DESIGNATES DC RETURN
6. FOR COMPLETE REFERENCE DESIGNATOR PREFIX WITH 2A1A13

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Figure 2-13. Storage tube protect, loads, and video amplifier 2A1A13, schematic diagram.

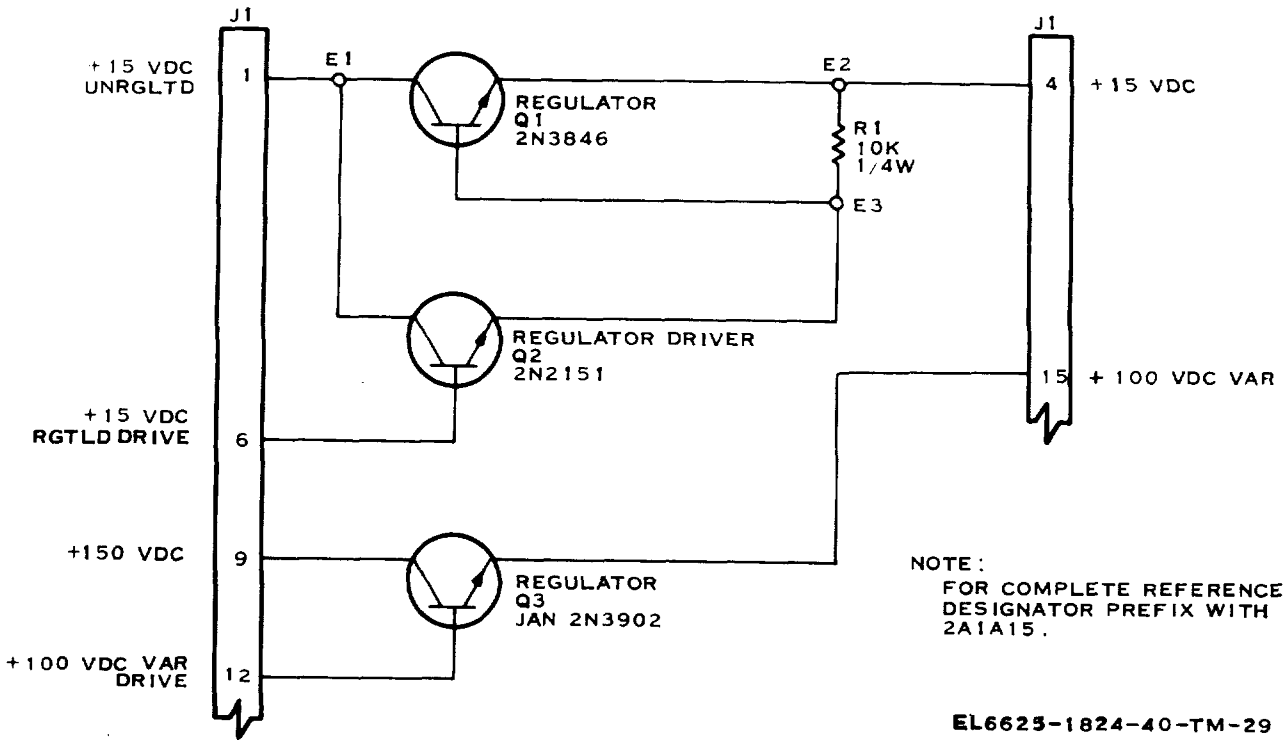


Figure 2-14. Heatsink assembly 2A1A15, schematic diagram.

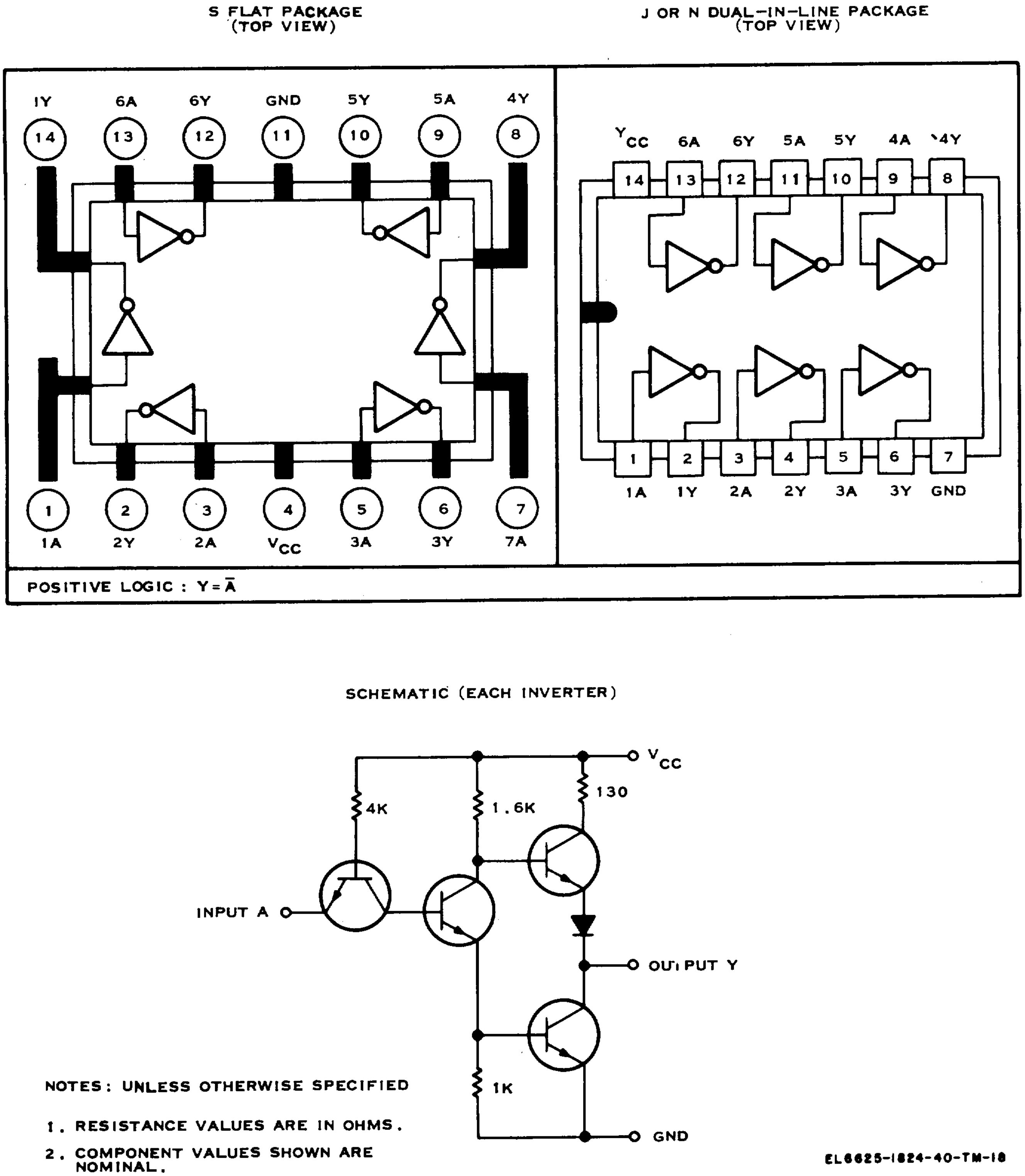


Figure 2-15. Integrated circuit, type SN5404.

CHAPTER 3

GENERAL SUPPORT MAINTENANCE

Section I. GENERAL

3-1. Level of Maintenance

This chapter provides general support maintenance procedures for Test Set, Converter Subassembly-Video Converter AN/AAM-35. Included in this chapter are sections covering: troubleshooting; removal and replacement; adjustment and alignment; repair; and general support testing.

3-2. Maintenance Forms and Records

Maintenance forms, records and reports which are to be used by maintenance personnel at all maintenance levels are listed in and prescribed by TM 38-750.

3-3. Tools and Test Equipment

Tools and test equipment required for maintenance, other than those listed in TM 11-66251824-12, are as follows:

a. Tools. The only tools required are a 55-watt soldering iron and Tool Kit, Electronic TK-105/G.

b. Test Equipment. Test equipment is listed in table 3-1.

Table 3-1. Test Equipment

Nomenclature	*Common Name*
Oscilloscope AN/USM-281	Oscilloscope
Digital Voltmeter, Non-Linear Systems, Model X-2	Digital Voltmeter (dvm)
Multimeter, TS-352B/U	Multimeter
Tool Kit, Electronic Equipment TK-100/G.	Tool kit
Maintenance Kit, Electronic Equipment MK-1172/ AAS-24	Electronic maintenance kit
Function Generator, Wavetek Model 111 (SG-769/U).	Function generator
Electronic Counter, Hewlett-Packard Model 5245L (CP 772/U)	Frequency counter

c. Digital Voltmeter Preparation for Use. To prepare the digital voltmeter (dvm) for use, connect the power plug to a 115-vac power source (fig. 3-1). Connect the red lead to the HI connector on the dvm panel and the black lead to the LO connector on the dvm panel. Set the power switch to ON. Set the range switch to

AUTO.

d. Oscilloscope Preparation for Use. To prepare the oscilloscope for use, connect the power lead to 115-vac power source (fig. 3-1). Connect the oscilloscope test probe to INPUT CH 1. Make a connection between ground on the oscilloscope and GND on control unit 1Al. Set the POWER ON switch to the ON position. Position controls as indicated in chart 3-1.

Chart 3-1. Oscilloscope AN/USM-281A Control Settings.

Controls	*Settings*
FIND BEAM	Released.
INTENSITY	As required.
ASTIOGMATISM	Use in conjunction with FOCUS to adjust for round beam.
FOCUS	Adjusts beam for sharpest trace.
TRACE ALIGN	Adjusts vertical centering.
SCALE	Adjusts for scale illumination.
POWER (indicator)	Signifies POWER switch closed and the 23-vdc power supply is operating.
POWER (switch)	ON (applies ac power to oscilloscope).
HORIZONTAL POSITION	Adjusts horizontal position of display.
DISPLAY	INT.
AC DC	DC.
A POSITION	As required.
POLARITY	+UP.
DISPLAY	A.
VOLTS/CM	1.
MAGNIFIER	X1.
CH 1 AC GND DC INPUT	DC.

Chart 3-1. Oscilloscope AN/USM-281A Control Settings-Continued

Controls	*Setting*
MAIN VERNIER	CAL.
RESET	Released.
TRIGGER LEVEL	0.
EXT ÷ 10, EXT, INT, LINE	INT.
-SLOPE +	+
ACS, ACF, AC, DC	DC.
TIME/CM	1 µsec.

Chart 3-1. Oscilloscope AN/USM-281A Control Settings-Continued

Controls	*Setting*
SWEEP MODE	AUTO.
CM DELAY	0.
VERNIER	CAL.
TRIGGER LEVEL	0.
INT, AUTO, EXT, EXT ÷ 10	AUTO.
-SLOPE +	+.
ACS, ACF, AC, DC	DC.

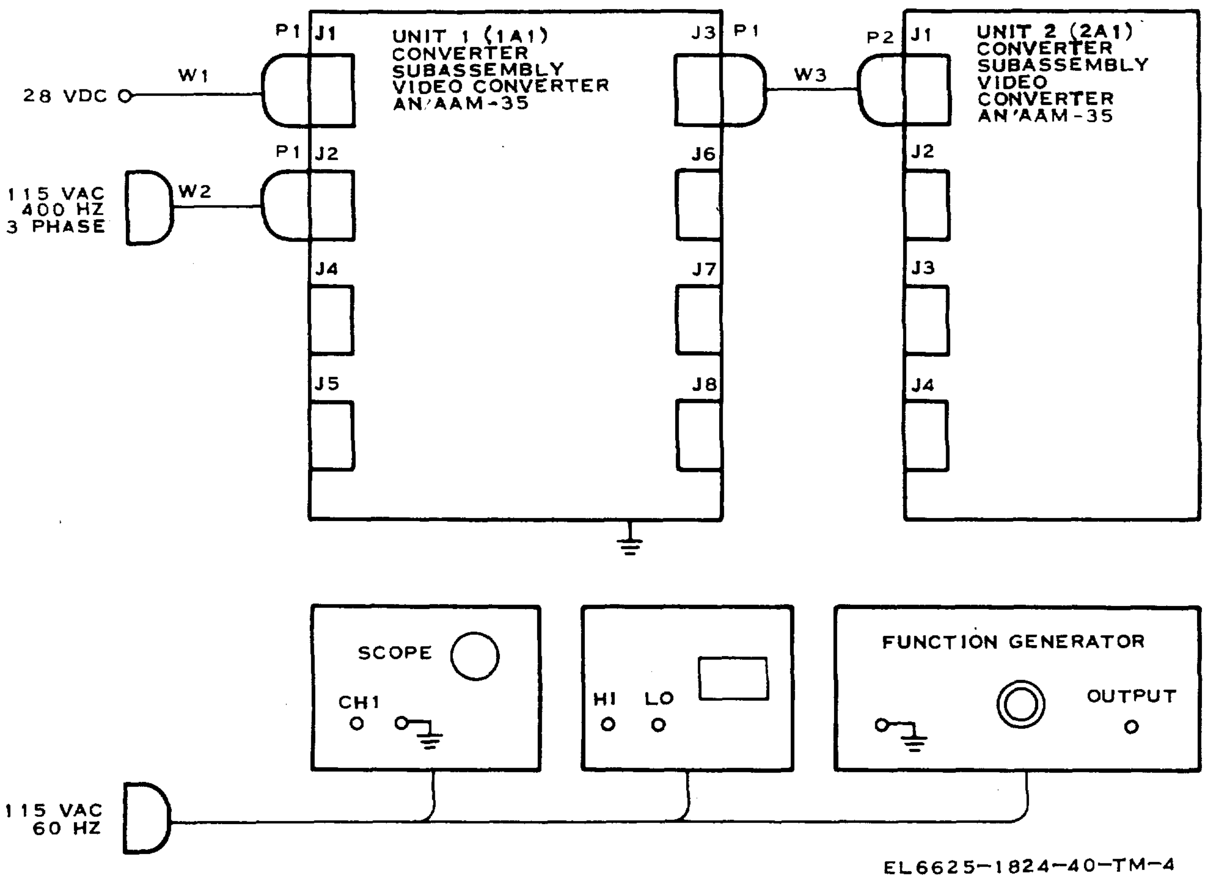


Figure 3-1. Test setup.

Section II. TROUBLESHOOTING

3-4. General Troubleshooting Instructions

Troubleshooting at the general support maintenance level includes all the techniques outlined for organizational maintenance, and any special or additional techniques required to isolate a defective part. The maintenance procedures are not complete in themselves, but supplement those described in TM 11-6625-1824-12. The systematic troubleshooting procedure, which begins with the operational and sectionalization checks that are performed at an organizational level, must be completed by means of localizing and isolating techniques. The paragraphs that follow provide procedures for sectionalizing troubles to a particular functional unit of the test set, and then to localize the trouble to a component of the functional unit unless the functional unit is replaced and later repaired at a higher level maintenance facility. Waveforms are provided in figure 3-2. Parts location information is provided in figures 3-3 and 3-4. Wiring diagram information and cable diagrams are provided in figures FO-7, FO-8, and FO-9. Color codes for resistors, inductors, and capacitors is provided in figure FO1. The color code for wire shown on wiring diagrams is the same numerical code explained in figure FO-1.

3-5. Organization of Troubleshooting

a. General. The first step in troubleshooting is to sectionalize the fault (tracing the fault to a major functional unit). The second step is to localize the fault (tracing the fault to a defective part within that unit). Some faults, such as burned-out resistors, arcing, and shorted transformers can often be located by sight, smell, and hearing. The majority of faults, however, must be isolated by checking voltages and resistances, or by checking the equipment against the general support test procedure contained in section VI of this chapter.

b. Sectionalization. For ease of troubleshooting, the equipment may be thought of as consisting of functional entities, each related electrically but categorized separately by the function performed. The first step in troubleshooting is to locate the function, or functions, at fault by the following methods:

(1) *Visual inspection.* The purpose of the visual inspection is to locate faults without testing or measuring 'the circuits. All visual signs should be observed and an attempt made to sectionalize the fault to a particular function.

(2) *Operational test.* Operational tests frequently indicate the general location of trouble. In many instances the tests will help in determining the exact nature of the fault. The organizational quarterly preventive maintenance checks and service chart (TM 11-6625-1824-12) contains an operational test.

c. Localization. The tests listed in the following paragraphs will aid in localizing the trouble. First, localize the trouble to a single function, and then isolate the trouble within that circuit by waveform, resistance, and continuity measurements.

(1) *Troubleshooting chart*. When used with the associated voltage, resistance, and continuity tables and the waveform diagram, the troubleshooting information in chart 3-1 will aid the technician in localizing troubles to a component part. Defective components identified by performing the corrective action are replaced with a known reliable component unless repair or other disposition is noted. The corrective action column reference data tables, if required, for checking components; otherwise, refer to schematics and wiring diagrams when performing checks. The parenthetical reference in the malfunction column is intended to be used only when performing the general support test procedure. The referenced data items and test procedure steps will allow malfunction symptoms discovered during performance of the test procedure to be easily referenced in the troubleshooting chart.

Chart 3-2. Troubleshooting Procedure

	Malfunction	*Probable cause*	*Corrective action*
1.	FAIL lamp 1A1DS1 lights when power mode switch 1A1S1 is set to STBY.	*a*. Loss of 115-vac input power.	*a*. Check CB2. Reset if tripped.
		b. 115-vac, 400-Hz, 3-phase input	*b*. Check input 115-vac, 400 Hz, incorrect. 3-phase.
		c. Power fluctuation. RESET and release.	*c*. Set power mode switch to
		d. No input to power transformer 1A1T1.	*d*. Check standby relay 1A1K1 (table 3-3, item 1).
		e. Output of transformer 1A1T1 incorrect.	e. Check output of transformer 1A1T1 (table 3-2, items 4 through 18).
		f. Input to power control lA1A6 incorrect.	*f*. Perform the following:
		(1) +15 vdc at 1A1A6-16 incorrect.	(1) Check 2A1A14-1 for +15 ±0.3 vdc. If present, check 2A1A15-15 for 15 ±0.3 vdc. If present check continuity.
		(2) +5 vdc at 1A1A6-14 incorrect.	(2) Check 1A1A2-1 for +5 ±0.1 vdc. If present check 1AK5-A1 for +5 ±0.1 vdc.
		(3) -15 vdc at 1A1A6-17 incorrect.	(3) Check 1A1A1-6 for -15 ±0.3 vdc.
		(4) +150 vdc at 1A1A6-18 incorrect.	(4) Check 1A1A4-16 for + 150 ±3 vdc. If incorrect, check 1A1A3-16 for +250 ±5.0 vdc.
		(5) +250 vdc at 1A1A6-5 incorrect.	(5) Check 1A1A3-16 for 250 ±5.0 vdc.
		g. Power control 1A1A6 defective.	*g*. Check 1A1A6.

Chart 3-2. Troubleshooting Procedure-Continued

Malfunction	Probable cause	Corrective action
2. ELAPSED TIME meter 1A1M1 does not operate with power mode switch 1A1S1 in STBY or OPR. FAIL lamp is not lighted.	ELAPSED TIME meter 1A11M1, or wiring defective.	Check 1A1M1 and wiring.
3. STBY lamp 1A11DS2 does not light when power mode switch 1A1S1 is in STBY. Fail lamp is extinguished.	*a*. Defective circuit breaker 1A1CB1.	*a*. Check 1A1CB1.
	b. Diode 1A10R1 open.	*b*. Check 1A1CR1 (table 3-2, items 19 and 20).
	c. Standby relay 1A1K1 defective.	*c*. Check 1A11K1 (table 3-3, item 1).
	d. Power mode switch 1A1S1 defective.	*d*. Check 1A1S1 (table 3-4, items 7, 8 and 9).
	e. STBY lamp defective.	*e*. Check 1A1DS1.
4. OPR lamp 1A1DS3 does not light with power mode switch 1A1S1 in OPR. FAIL lamp 1A1DS1 is not lighted.	*a*. Operate relay 1A1K2 defective.	*a*. Check 1A1K2 (table 3-3, item 1).
	b. OPR lamp 1A1DS3 defective.	*b*. Check 1A1DS3.
5. No 115 vac, 3 phase, 400 Hz at 2A1lJ3-A, B and C. 115 vac, 3 phase, 400 Hz is present at 1A1J5J, K and L.	Defective transfer relay 2A1K1.	Check 2A1K1.
6. Missing one or more phases of 115 vac, 3 phase 400 Hz at 1A1J5J, K and L.	*a*. Defective operate relay coil 1A1K2	*a*. Check 1A1K2 coil (table 3-3, item 1).
	b. Defective operate relay 1A1K2 contacts.	*b*. Check 1A1K2 contacts for continuity.
7. -15 vdc not in tolerance at 2A1J3-DD.	*a*. Defective power transformer 1A1T1.	*a*. Check 1A1T1 output (para 3-5.c. (3); table 3-2, items 7, 8 and 9).
	b. Defective -15-vdc power supply 1A1A1.	*b*. Check 1A1A1-6, 13 for -15 ±0.3 vdc.
	c. Defective power relay 1A1K3.	*c*. Check 1A1K3-B1 for 4510.3 vdc.
	d. Defective transfer relay 2A1K3.	*d*. Check 2A1K3-A1 for -1510.3 vdc.
8. +5 vdc not in tolerance at 2A1J3-CC.	*a*. Defective power transformer 1A1T1.	*a*. Check 1A1T1 output (table 3-2, items 13, 14 and 15).
	b. Defective ic power supply 1A1A2.	*b*. Check 1A1A2-1, 3 for +5 ±0.5 vdc.
	c. Defective phase sensing relay 1A1K5.	*c*. Check 1A1K5-A2 for +5 ±0.5 vdc. Check A, B and C input for 115 ±11.5 vac.
	d. Defective power relay 1A1K3.	*d*. Check 1A1K3-A1 for +5 ±00.5 vdc.
	e. Defective transfer relay 2A1K2.	*e*. Check 2A1K2-C1 for +5 ±0.5 vdc.
9. +250 vdc not in tolerance at 2A1J3-GG.	*a*. Defective power transformer 1A1T1.	*a*. Check 1A1T1 output (table 3-2, items 10, 11 and 12).
	b. Defective +250 vdc power supply 1A1A3.	*b*. Check output of 1A1A3-16 for +250 ±5.0vdc.
	c. Defective heatsink 1A1A14.	*c*. Check output of 1A1A14-3 for 250 ±5.0 vdc.
10. + 150 vdc not in tolerance at 2A1J3-FF.	*a*. Defective +250 vdc power supply 1A1A3.	*a*. Refer to 9 above.
	b. Defective 150 vdc power supply	*b*. Check 1A1A4-16 for +,150 ±1.0 vdc. 1A1A4.
	c. Defective power relay 1A1K4.	*c*. Check 1A1K4-A1 for + 150 ± 1.0 vdc.
	d. Defective transfer relay 2A1K3.	*d*. Check 2A1K3-B1 for 150 ± 1.0 vdc.
11. +15 vdc not in tolerance at 2A1J3-EE	*a*. Defective power transformer	*a*. Check 1A1T1 output (table 3-2,
	b. Defective +15 vdc power supply 2A1A14.	*b*. Check 2A1A14-2 for +15 ±0.3 vdc.
	c. Defective heatsink 2A1A15.	*c*. Check 2A1A15-4 for +15 ±0.3 vdc.
	d. Defective power relay 1A1K4.	*d*. Check 1A1K4-C1 for +15 ±0.3 vdc.
	e. Defective transfer relay 2A1K2.	*e*. Check 2A1K2-D1 for +15 ±0.3 vdc.
12. +6.3 vdc not in tolerance at 2A1J3-K.	*a*. Defective power transformer 1A1T1.	*a*. Check 1A1T1 output (table 3-2, items 16, 17 and 18).
	b. Defective storage tube filament supply 1A1A5.	*b*. Check 1A1A5-2 for +16 ±0.01 vdc.
	c. Defective heatsink 1A1A13.	*c*. Check 1A1A13-23 for +6.:3 ±0.01 vdc.

Chart 3-2. Troubleshooting Procedure-Continued

Malfunction	*Probable cause*	*Corrective action*
12. (Contd)	*d.* Defective power relay 1A1K3.	*d.* Check 1A1K3-C1 for +613 ±0.01 vdc.
	e. Defective transfer relay 2A1K2.	*e.* Check 2A1K2-A1 for +6.3 ±0.01 vdc.
13. Video gate and video gate waveforms at 1A1J7-1A1J7-H And J respectively incorrect (chart 3-3, steps 11 and 12).	*a.* Defective signal generator 2A1A1.	*a.* Check 2A1A1-21 for waveform K, figure 3-2.
	b. Defective simulator 1A1A7.	*b.* Check 1A1A7-23 or 8 for waveform A, or B respectively, figure 3-2.
14. Simulated video waveform at test point TEST 4 incorrect (chart 3-3, step 13).	*a.* Defective signal generator 2A1A1.	*a.* Check 2A1A1-21 for waveform A, figure 3-2.
	b. Defective simulator 1A1A7.	*b.* Check 1A1A7-1 for waveform C, figure 3-2.
15. Video No. 1 waveform incorrect at test point TEST 7 (chart 3-, step 14).	*a.* Defective simulated video input from cs-vc simulator 1A1A7.	*a.* Check input at 1A1A8-15 or test point TEST 4 for waveform C, figure 3-2.
	b. Defective VIDEO/SIM TEST switch 1A1S2.	*b.* Check 1A1S2 (table 3-4, items 10 and 11).
	c. Defective video interface 1A1A8.	*c.* Check 1A1A8-7 (TEST 7), waveform I), figure 3-2.
16. Video No. 2 waveform incorrect at test point TEST 8 (chart 3-3, step 15).	*a.* Defective simulated input video from cs-vc simulator 1A1A7.	*a.* Check input at 1A1A8-15 or TEST 4, Waveform C, figure 3-2.
	b. Defective VIDEO/SIM TEST switch 1A1S2.	*b.* Check 1A1S2 (table 3-4, items 10 and 11).
	c. Defective video interface 1A1A8.	*c.* Check 1A1A8-9 (TEST 8) for waveform E, figure 3-2.
17. Velocity/height field of view incorrect at test point 9 (chart 3-3, step 16).	*a.* Incorrect input to sync interface 1A1A9.	*a.* Check inputs 1A1A9-18, 21.
	(1) FIELD OF VIEW: 1/4	(1) 1A1A9-18: 0.0 1A1A9-21: 0.0
	(2) FIELD OF VIEW: 1/2	(2) 1A1A9-18: 0.0 1A1A9-21: -15 ±0.3 vdc
	(3) FIELD OF VIEW: FULL	(3) 1A1A9-18: -15 ±0.3 vdc 1A1A9-21: -15 ±0.3 vdc
	b. Defective sync interface 1A1A9.	*b.* Replace 1A1A9.
18. Video gate waveform incorrect at test point CRT (chart 3-3, step 17).	*a.* Defective simulator 1A1A7.	*a.* Check 1A1A7-23 output (1A1J7-H) for waveform A, figure 3-2.
	b. Defective sync interface 1A1A9.	*b.* Replace 1A1A9.
19. Hot target waveform incorrect at test point TEST 6 (chart 3-3, step 18).	*a.* Refer to 18.a.	*a.* Refer to 18.a.
	b. Refer to 18.b.	*b.* Check 1A1A9-11 for waveform G, figure 3-2.
	c. Defective hot target and slew voltage generator 1AlA10.	*c.* Check 1A1A10-6 for waveform J, figure 3-2 and 1A1A10-8 for waveform I, figure 3-2.
	d. Defective sync interface 1A1A9.	*d.* Replace 1A1A9.
20. Hot target waveform incorrect at test point TEST 5 (chart 3-3, step 19).	*a.* Defective sync interface 1AIA9.	*a.* Check 1A1A9-11 for waveform G, figure 3-2.
	b. Defective hot spot and slew voltage generator 1A1A10.	*b.* Replace 1A1A10.
21. 100 kHz waveform at test point CRT incorrect (chart 3-3, step 21).	Defective signal generator, 2A1A1.	Check 2A1A1-23 for waveform K, figure 3-2.
22. Read horizontal sync waveform at test point HORIZ SWP incorrect (chart -3, step 22). HORIZ SWEEP 2A1S3: RD HORIZ SYNC.	*a.* Defective signal generator 2A1A1.	*a.* Check 2A1A1-23 for waveform K, figure 3-2.
	b. Defective sync generator 2A1A2.	*b.* Replace 2A1A2.
23. Read vertical sweep waveform at test point VERT SWP incorrect (chart 3-3, step 23), VERT SWEEP 2A1S1: RD SWP V.	*a.* Refer to 22.a. above.	*a.* Refer to 22.a. above.
	b. Defective sync generator 2A1A2.	*b.* Check 2A1A2 for waveform Y, figure 3-2.
	c. Defective read vertical sweep generator.	*c.* Replace 2A1A3.

Chart 3-2. Troubleshooting Procedure-Continued

Malfunction	Probable cause	Corrective action
24. Write horizontal sweep waveform at test point HORIZ SWP incorrect (chart 3-3, step 24). HORIZ SWEEP 2A1S3: WRT SWP. SLEW 2A1S7: 0°. FIELD OF VIEW 2A1S6: FULL.	*a.* Refer to 18.a.	*a.* Refer to 18.a.
	b. Refer to 18.b.	*b.* Check 1A1A9-7 (TEST 3) for waveform G, figure 3-2.
	e. Defective write horizontal sweep generator 2A1A4.	*c.* Check 2A1A4-tp 4 for waveform Z, figure 3-2.
	d. Defective write horizontal sweep generator 2A1A4.	*d.* Check 2A1A4-6 (test point 2) for dvm reading of 5.25 ±0.01 vdc.
	e. Defective resistor network 2A1R14 through R20.	*e.* Check FIELD OF VIEW 2A1S6C-7 (test point 1) for 3.0 ±0.2 vdc.
	f. Defective FIELD OF VIEW switch 2A1S6.	*f.* Check inputs 2A1A5-11 and 15 for -15 ± 0.3 vdc.
	g. Defective write horizontal slew and fov adder 2A1A5.	*g.* Replace 2A1A5.
25. Write horizontal sweep waveform at test point HORIZ SWP incorrect (chart 3-3, step 25). SLEW 2A1S7: 0°. FIELD OF VIEW 2A1S6:	*a.* Refer to 24.a. through e.	*a.* Refer to 24.a. through c.
	b. Defective FIELD OF VIEW switch 2A1S6.	*b.* Check inputs 2A1A-1 for -15 ±0.3 vdc and 2A1A-15 for 0.0 ±0.3 vdc.
	c. Defective write horizontal slew 1/12.	*c.* Replace 2A1A5. and fov adder, 2A1AS.
26. Write horizontal sweep waveform at test point HORIZ SWP incorrect (chart 3-3, step 26). SLEW 2A1S7: LEFT 30°. FIELD OF VIEW 2A1S6: 1/4.	*a.* Refer to 24.a. through e.	*a.* Refer to 24.a. through e.
	b. Defective FIELD OF VIEW switch 2A1S6.	*b.* Check inputs 2A1A5-11 and 15 for 0.0 °0.3 vdc.
	c. Defective SLEW switch 2A1S7.	*c.* Check 2A1S7 wiper (test point 1) for 5.25 ±0.01 vdc.
	d. Defective write horizontal slew and fov adder 2A1A6.	*d.* Replace 2A1A5.
27. Write horizontal sweep waveform at test point HORIZ SWP incorrect (chart 3-3, step 27). SLEW 2A1S7: RIGHT 30°. FIELD OF VIEW 2A1S6: 1/4.	*a.* Refer to 26.a. and b.	*a.* Refer to 26.a. and b.
	b. Defective SLEW switch 2A1S7.	*b.* Check 2A1S7 wiper (test point 1) for 0.75 °0.05 vdc.
	c. Defective write horizontal slew and fov adder 2A1A5.	*c.* Replace 2A1A5.
28. Write composite blanking waveform at test point INPUT C incorrect (chart 3-3, step 28). INPUTS 2A1S8: 01.	*a.* Refer to 24, 25, 26 or 27 dependent on FIELD OF VIEW 2A1S6 and SLEW 2A1S7 settings as shown in each step.	*a.* Refer to 24, 25, 26 or 27 dependent on FIELD OF VIEW 2A1S6 and SLEW 2A1S7 settings as shown in each step.
	b. Refer to 23.b.	*b.* Refer to 23.b.
	c. Defective v/h clock pulse generator 2A1A7.	*c.* Check 2A1A7-16 for waveform AA, figure 3-2.
	d. Defective write vertical sweep generator 2A1A8.	*d.* Check 2A1A8S-8 for waveform AC, figure 3-2.
	e. Defective v/h clock pulse generator 2A1A6.	*e.* Check 2A1A7-8 for waveform AR, figure 3-2.
	f. Defective write horizontal slew and fov adder 2A1A5.	*f.* Replace 2A1A6.
29. Write video waveform incorrect at test point VIDEO (chart 3-3, step 29). VIDEO: WRT VID.	*a.* Refer to 17.a. and b.	*a.* Refer to 17.a. Check 1A1A9-20 (test point 9) for waveform F, figure 3-2.
	b. Defective auxiliary deflection logic 2A1A10.	*b.* Check 2A1A10-tp2 for waveform AD, figure 3-2.
	c. Refer to 15 and 16a. through .	*c.* Refer to 15 and 16 a. through e.
	d. Defective write video amplifier 2A1A6.	*d.* Replace 2A1A6.
30. Write vertical sweep waveform at test point VERT SWP incorrect (chart 3-3, step 30). VERT SWP: WRT COMP WP V. TUBE PROTECT/ FRAME HOLD switch to TUBE PROTECT .	*a.* Refer to 24.b.	*a.* Refer to 24.b.
	b. Defective write horizontal sweep generator 2A1A4.	*b.* Check 2A1A4-18 for waveform AE, figure 32.
	c. Defective write vertical sweep generator 2A1A8.	*c.* Check 2A1J3-u for waveform AF, figure 3-2.
	d. Defective erase vertical sweep generator 2A1A9.	*d.* Replace 2A1A9.

Chart 3-2. Troubleshooting Procedure-Continued

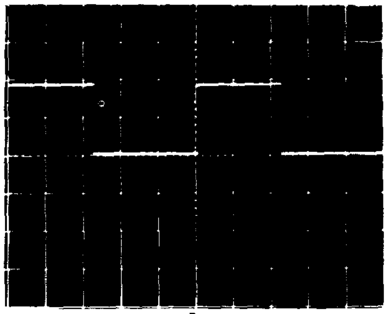
Malfunction	Probable cause	Corrective action
31. Dither waveform at 2A1J4-c incorrect (chart 3-3, step 31). logic 2A1A10.	*a.* Refer to 29.a.	*a.* Refer to 29.a.
	b. Defective auxiliary deflection	*b.* Check 2A1A10-9 for waveform AG, figure 3-2.
	c. Defective dither generator 2A1A11.	*c.* Replace 2A1A11.
32. Horizontal sweep waveform incorrect at test point X OSCP (chart 3-3, step 32).	*a.* Refer to 22.a.	*a.* Refer to 22.a.
	b. Defective sync generator 2A1A2.	*b.* Check 2A1A2-2 for waveform AH, figure 3-2.
	c. Defective sweep and blanking 2A1A12.	*c.* Replace 2A2A12.
33. Vertical sweep waveform incorrect at test point Y OSCP (chart 3-3, step 33).	*a.* Refer to 32.a. and b.	*a.* Refer to 32.a. and b.
	b. Defective sync generator 2A1A2.	*b.* Check 2A1lA2-1 for waveform Y, figure 3-2.
	c. Defective VERT SYNC TEST switch 2A1S12.	*c.* Check 2A1S12 (table 3-4, items 184 and 185).
	d. Defective sweep and blanking 2A2A12.	*d.* Replace 2A1A12.
34. Read video amplified and blanked waveform incorrect at test point Z OSCP (chart 3-3, step 34). figure 3-2.	*a.* Test setup. generator settings.	*a.* Check connections and function
	b. Defective sweep and blanking 2A1A12.	*b.* Check 2A1A12-5 (test point: 3 on 2A1A12) for waveform AT,
	c. Defective storage tube protect, loads and video amplifier 2A1A13.	*c.* Replace 2A1A13.

(2) *Waveform measurements (fig. 3-1)* Oscilloscope AN/USM-281A is used for observing waveforms at appropriate test points. The waveform chart on figure 3-2 illustrates the waveforms obtained at various points on the chassis.

(3) *Voltage and resistance measurements*. The digital voltmeter, Nonlinear System, Model X-2 , is used for taking voltage and resistance measurements on the chassis. Multimeter TS352B/U is available if required. Voltage measurements are listed in table 3-2 and resistance measurements are listed in table 3-3. The item column is provided so specific measurements can be easily referenced. The component checked column designates which component can be checked by using the data provided for that item. The dvm probe connections LO and HI columns specify where the HI probe and LO probe are connected to check the corresponding item component. The test set control setting control and position columns designate test unit control settings which must be made prior to observing the dvm indication for the item checked. The dvm indication (volts) dc and ac column on the voltage measurement table (table 3-2) contains the dvm dc or ac voltage obtained for the item component checked. The dvm indication (ohms) on the resistance measurement table (table 3-3) contains the resistance obtained for the item checked. Unless otherwise specified, tolerances are ±10 percent. Chassis mounted components requiring resistance checks must be isolated from associated circuitry to avoid erroneous readings.

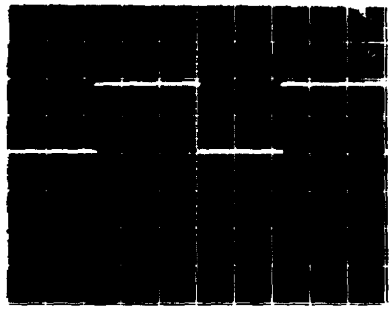
CAUTION

When making voltage measurements of transistors, use tape or sleeving to insulate the test probe, except for the extreme tip, to prevent accidental shorting of the test probes to the chassis (even a momentary short circuit can damage the transistor).



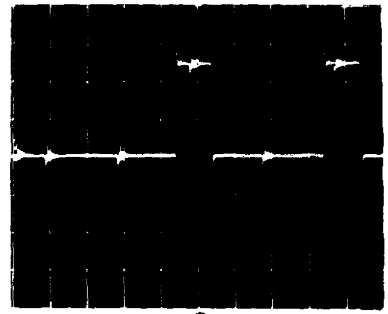
A

VIDEO GATE FROM 1A1A7-23
TO 1A1J7-H
OSCILLOSCOPE:
SWEEP - 1 MS/CM
SENSITIVITY - 2.0V/CM



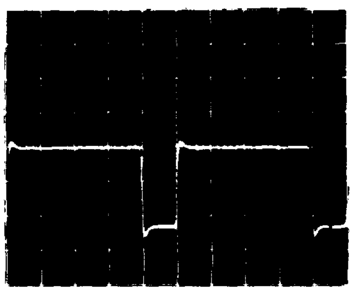
B

VIDEO GATE FROM 1A1A7-8
TO 1A1J7-J
OSCILLOSCOPE:
SWEEP - 1 MS/CM
SENSITIVITY - 2.0V/CM



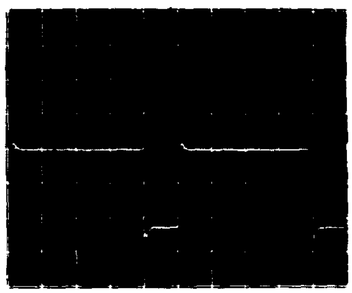
C

SIMULATED VIDEO FROM
1A1A7-1 TO TEST POINT
TEST 4
OSCILLOSCOPE:
SWEEP - 5µS/CM
SENSITIVITY 0.5V/CM



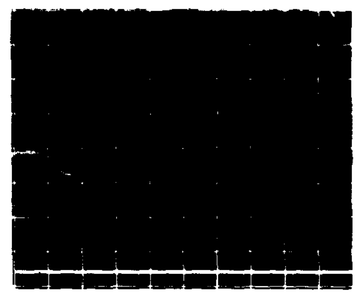
D

VIDEO NO.1 FROM 1A1A8-7
TO TEST POINT TEST 7
VIDEO/SIM TEST:
SIM TEST
OSCILLOSCOPE:
SWEEP - 5µS/CM
SENSITIVITY 0.5V/CM



E

VIDEO NO.2 FROM 1A1A8-9
TO TEST POINT TEST 8
OSCILLOSCOPE:
SWEEP - 5µS/CM
SENSITIVITY 0.5V/CM



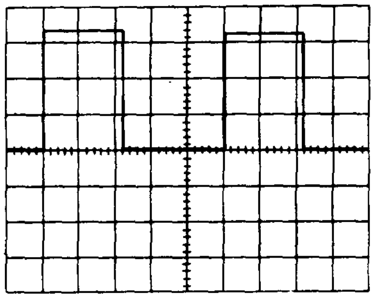
F

V/H FIELD OF VIEW FROM
1A1A9-20 TO TEST POINT 9.
OSCILLOSCOPE:
SWEEP - 5µS/CM
SENSITIVITY 1.0V/CM

OBSERVE NEGATIVE
DC VOLTAGE LEVEL
-1.8 TO -7.2 VOLTS DC

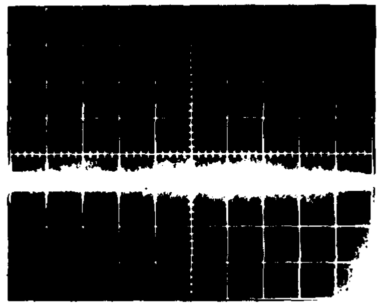
EL4IM001

Figure 3-2(1). Waveforms (part 1 of 7).



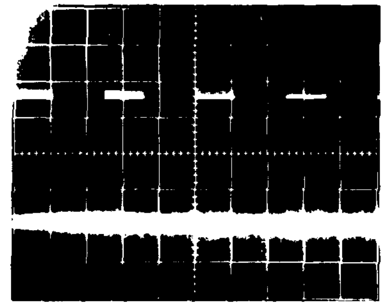
G

VIDEO GATE FROM 1A1A9–8
TO TEST POINT CTR
OSCILLOSCOPE:
SWEEP – 1 MS/CM
SENSITIVITY 1.0V/CM



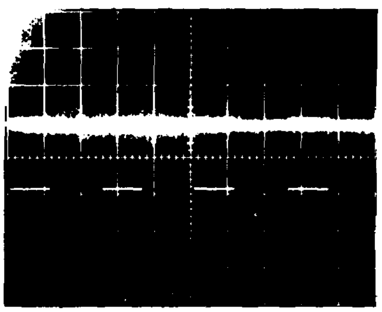
H

HOT TARGET FROM 1A1A9–6
TO TEST POINT TEST 6
HOT SPOT: ON
OSCILLOSCOPE:
SWEEP – 2MS/CM
SENSITIVITY 5V/CM



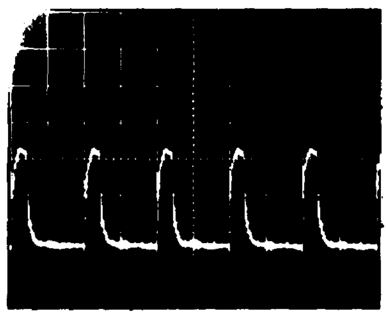
I

HOT TARGET FROM 1A1A10–8
TO TEST POINT TEST 5
OSCILLOSCOPE:
SWEEP – 2MS/CM
SENSITIVITY 1.0V/CM



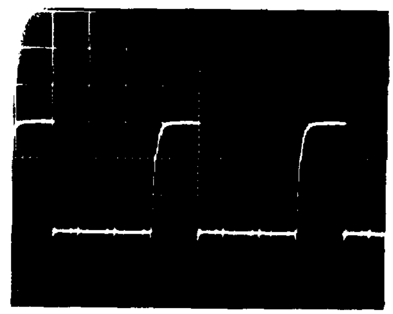
J

HOT TARGET FROM 1A1A10–6
TO 1A1J7–M
OSCILLOSCOPE:
SWEEP – 1 MS/CM
SENSITIVITY 1.0V/CM



K

100 KHZ FROM 2A1A1–23 TO
TEST POINT CTR
COUNTER: 100 KHZ OSC
OSCILLOSCOPE:
SWEEP
SENSITIVITY 2.0V/CM

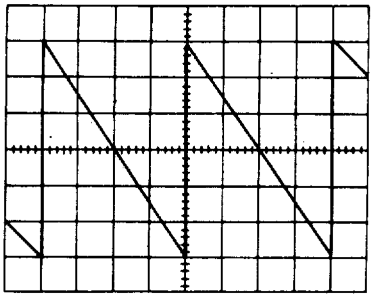


L

READ HORIZONTAL SYNC FROM
2A1A2–6 TO TEST POINT
HORIZ SWP HORIZ
SWEEP: RD HORIZ SYNC
OSCILLOSCOPE:
SWEEP – 1 MS/CM
SENSITIVITY 2.0V/CM

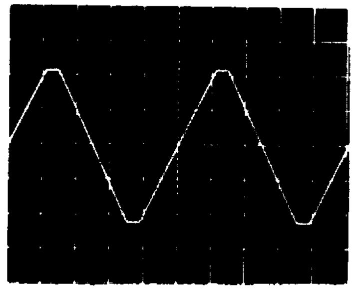
EL41M002

Figure 3-2(2). Waveforms (part 2 of 7)



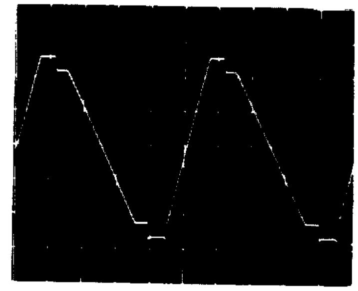
M

READ VERTICAL SWEEP FROM
2A1A3–6 TO TEST POINT
VERT SWP VERT
OSCILLOSCOPE:
SWEEP – 5 MS/CM
SENSITIVITY 2.0V/CM



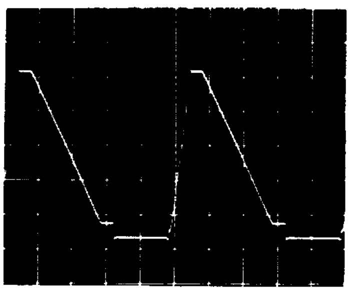
N

WRITE HORIZONTAL SWEEP
FROM 2A1A5–4 TO TEST
POINT
HORIZ SWP HORIZ
SWEEP: WRT SWP
SLEW: 0° FIELD OF
VIEW: FULL
OSCILLOSCOPE:
SWEEP – 1 MS/CM
SENSITIVITY 2.0V/CM



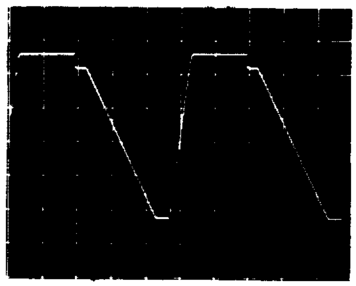
O

WRITE HORIZONTAL SWEEP
FROM 2A1A5–4 TO TEST
POINT
HORIZ SWP SLEW: 0
FIELD OF VIEW: 1/2
OSCILLOSCOPE:
SWEEP – 1 MS/CM
SENSITIVITY 2.0V/CM



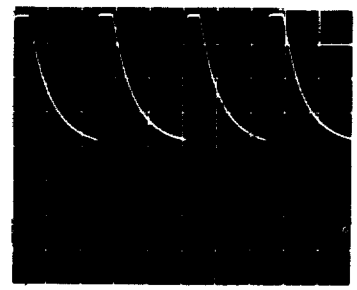
P

WRITE HORIZONTAL SWEEP
FROM 2A1A5–4 TO TEST
POINT
HORIZ SWP SLEW:
L 30 ; FIELD OF VIEW:
1/4
OSCILLOSCOPE:
SWEEP – 1 MS/CM
SENSITIVITY 2.0V/CM



Q

WRITE HORIZONTAL SWEEP
FROM 2A1A5–4 TO TEST
POINT
HORIZ SWP SLEW:
R 30° : FIELD OF VIEW:
1/4
OSCILLOSCOPE:
SWEEP – 1 MS/CM
SENSITIVITY 2.0V/CM

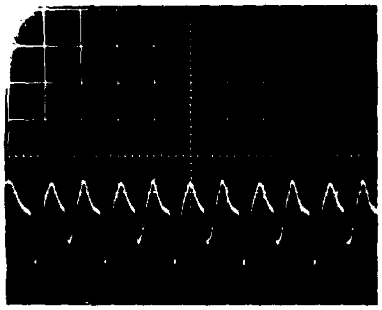


R

WRITE COMPOSITE BLANKING
FROM 2A1A5–8 TO TEST
POINT
INPUT C
OSCILLOSCOPE:
SWEEP – 1 MS/CM
SENSITIVITY 1.0V/CM

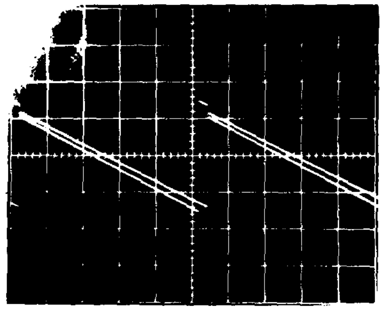
EL–6625–1824–40–C1–TM–15 (3)

Figure 3-2(3). Waveforms (part 3 of 7)



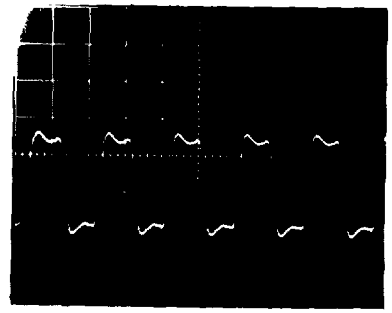
S

WRITE VIDEO FROM 2A1A6−14
TO TEST POINT VIDEO
VIDEO: HS MOD
OSCILLOSCOPE:
SWEEP −.5µS/CM
SENSITIVITY 1.0V/CM



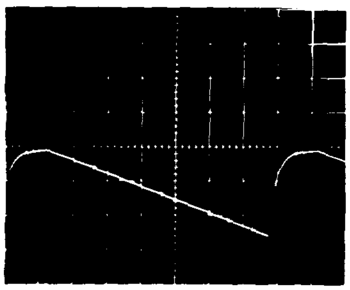
T

WRITE VERTICAL SWEEP
FROM 2A1A9−7 TO TEST
POINT
VERT SWP VERT SWP:
WRT COMP SWP V
OSCILLOSCOPE:
SWEEP − 0.5 S/CM
SENSITIVITY 2.0V/CM



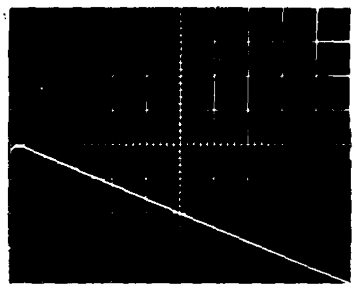
U

DITHER FROM 2A1A11−6 TO
2A1J4−c
OSCILLOSCOPE:
SWEEP−0.5 µS/CM
SENSITIVITY 0.2V/CM



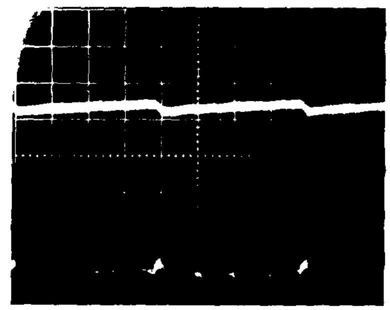
V

HORIZONTAL SWEEP FROM
2A1A12−23 TO TEST POINT
X OSCP
OSCILLOSCOPE:
SWEEP − 5µS/CM
SENSITIVITY 1.0V/CM



W

VERTICAL SWEEP FROM
2A1A12−1 TO TEST POINT
Y OSCP
OSCILLOSCOPE:
SWEEP − 2 MS/CM
SENSITIVITY 1.0V/CM

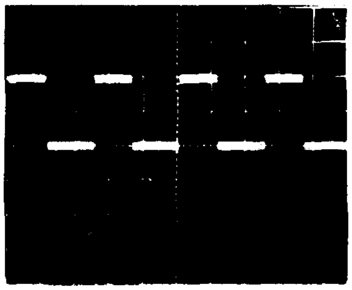


X

READ VIDEO AMPLIFIED AND
BLANKED FROM 2A1A13−9
TO TEST POINT
Z OSCP 100 KHZ
INSERTED AT 2A1J2−e
OSCILLOSCOPE:
SWEEP−5 MS/CM
SENSITIVITY 1.0V/CM
SYNC SCOPE AT Y OSCP

EL4IM003

Figure 3-2(4). Waveforms (part 4 of 7).

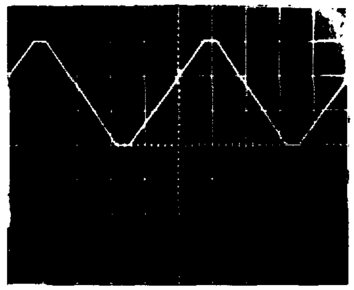


(Y)

VERTICAL SYNC FROM
2A1A2-1 TO 2A1J3-V

VERT SWEEP: RD SWP
V

OSCILLOSCOPE:
SWEEP-2 MSEC/CM
SENSITIVITY 2.0V/CM

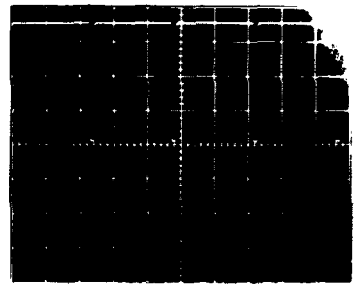


(Z)

WRITE HORIZONTAL SWEEP
FROM 2A1A4-4.

HORIZ SWEEP: WRT
SWP SLEW: 0° FIELD
OF VIEW: FULL

OSCILLOSCOPE:
SWEEP-1 MSEC/CM
SENSITIVITY 1.0V/CM

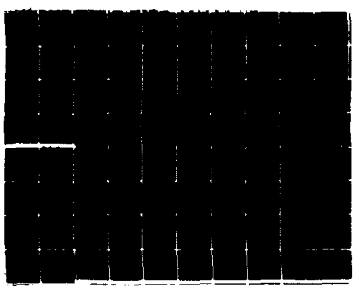


(AA)

CLOCK PULSE FROM
2A1A7-16. TAKEN AT
2A1A7-TP3 (ORN).

OSCILLOSCOPE:
SWEEP-1 MSEC/CM
SENSITIVITY 1.0V/CM

TUBE PROTECT/
FRAME HOLD: OFF
FIELD OF VIEW
(UNIT 1): FULL

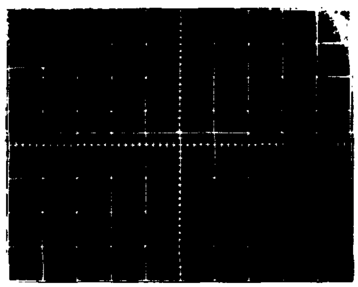


(AB)

WRITE VERTICAL BLANKING
FROM 2A1A7-8. TAKEN AT
2A1A7-TP2 (RED).

OSCILLOSCOPE:
SWEEP-0.2 MSEC/CM
SENSITIVITY 2.0V/CM

TUBE PROTECT/
FRAME HOLD: OFF
APPEARS ABOUT
EVERY 5 SECONDS.

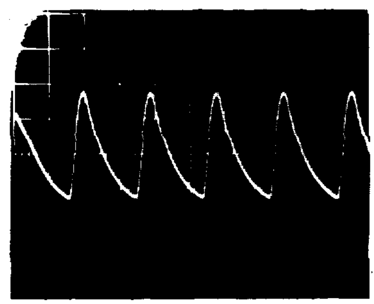


(AC)

4095 COUNT FROM
2A1A8-8

OSCILLOSCOPE:
SWEEP-1 MSEC/CM
SENSITICITY 2.0V/CM

TUBE PROTECT/
FRAME HOLD: OFF
APPEARS ABOUT
EVERY 5 SECONDS.



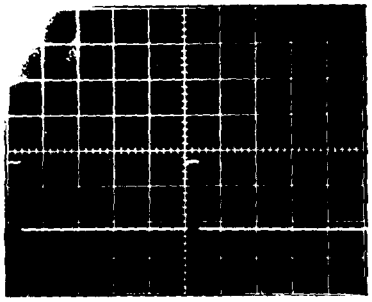
(AD)

SELECTOR CHOP FROM
2A1A10-4. TAKEN AT
2A1A10-TP2 (RED).

OSCILLOSCOPE:
SWEEP-2 MSEC/CM
SENSITICITY-1.0V/CM

EL4IM004

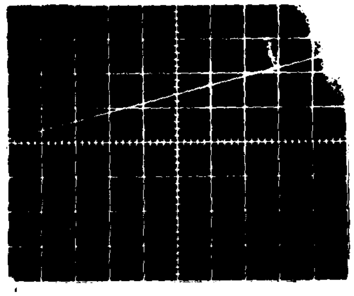
Figure 3-2(5). Waveforms (part 5 of 7)



(AE)

ERASE RETRACE PULSE FROM 2A1A4-18.

OSCILLOSCOPE:
SWEEP-1 MSEC/CM
SENSITIVITY 2.0V/CM



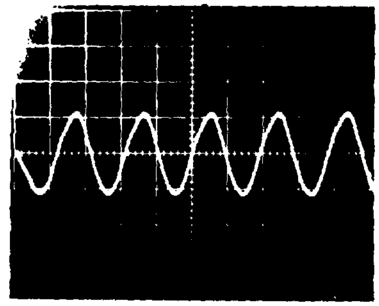
(AF)

WRITE VERTICAL RAMP FROM 2A1A8-4. TAKEN AT 2A1J3-u

VIDEO IN: CW VERT

SWEEP: WRT COMP SWP V

OSCILLOSCOPE:
SWEEP-1.0 SEC/CM
SENSITIVITY 2.0V/CM
FIELD-OF-VIEW (UNIT 1) TO FULL

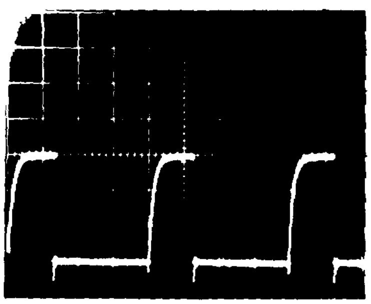


(AG)

CHOPPER DRIVE FROM 2A1A10-9

OSCILLOSCOPE:
SWEEP-2 MSEC/CM
SENSITIVITY 5.0V/CM

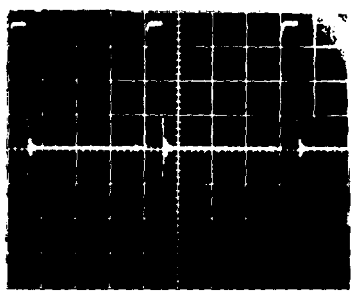
FIELD-OF-VIEW (UNIT 1): 1/4



(AH)

READ HORIZONTAL SYNC FROM 2A1A2-2. TAKEN AT 2A1A2-TP2 (RED).

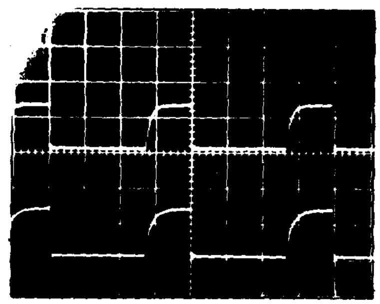
OSCILLOSCOPE:
SWEEP-10 μSEC/CM
SENSITIVITY 2.0V/CM



(AI)

BLANKING PULSE FROM 2A1A12-5. TAKEN AT 2A1A12TP2(RED). 100 KHZ INSERTED AT 2A1J2-e.

OSCILLOSCOPE:
SWEEP-10 μSEC/CM
SENSITIVITY 2.0V/CM



(AJ)

READ HORIZONTAL SYNC CH 1 FROM 2A1A2-6. TAKEN AT TEST POINT

HORIZ SWP. CH 2 TAKEN AT 2A1A2-TP1 (WHT).

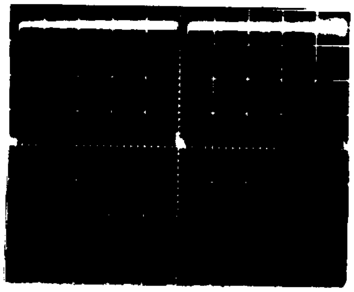
HORIZ SWEEP: RD HORIZ SYNC

OSCILLOSCOPE:
SWEEP-10 μS/CM
SENSITIVITY 5V/CM

EL4IM005

Figure 3-2(6). Waveforms (part 6 of 7)

OV



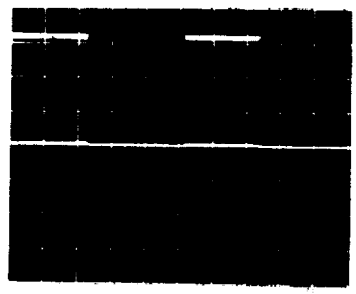
AK

CLOCK PULSE FROM
2A1A7-14

OSCILLOSCOPE:
SWEEP-0.5 MS/CM
SENSITIVITY 1.0V/CM

FIELD OF VIEW: FULL

CLOCK PULSE (2A1A7-14):
÷10 SAMPLE TAKEN AT
INPUT C TEST POINT; INPUTS 02



AL

GATED VIDEO FROM
2A1A1-1 TO TEST POINT
INPUT B INPUTS: 0.7
OSCILLOSCOPE:
SWEEP-1 MS/CM
SENSITIVITY 1.0V/CM

GATED VIDEO
(2A1A1-1):
TAKEN AT INPUT B TEST POINT,
INPUTS 07

AM

CHOPPED VIDEO
TAKEN AT VIDEO 2A1J7
VIDEO: AS MOD
OSCILLOSCOPE:
SWEEP 2 μS/CM
SENSITIVITY 1V/CM

EL4IM006

Figure 3-2(7). Waveforms (part 7 of 7).

Table 3-2. Voltage Measurements

Item	Component checked	Dvm probe connection		Test set control setting		Dvm indication (volts)	
		LO	HI	Control	Position	Ac	Dc
1.	1A1T1	1A1TB1-4	1A1TB1-1	Power mode	STBY	120 ± 24	
2.	1A1T1	1A1TB1-4	1A1TB1-2	Power mode	STBY	120 ± 24	
3.	1A1T1	1A1TB1-4	1A1TB1-3	Power mode	STBY	120 ± 24	
4.	1A1T1	2A1XA14-16	2A1XA14-10	Power mode (Insert extender board in 2A1XA14)	STBY	23.9 ± 5	
5.	1A1T1	2A1XA14-16	2A14L1-18	Power mode (Insert extender board in 2A1XA14)	STBY	23.9 ± 5	
6.	1A1T1	2A1XA14-10	2A1XA14-18	Power mode (Insert extender board in 2A1XA14)	STBY	23.9 ± 5	
7.	1A1T1	1A1XA1-16	1AXA1-18	Power mode (Insert extender board in 1A1XA1)	STBY	21.6 ± 4	
8.	1A1T1	1A1XA1-16	1A1XA1-10	Power mode (Insert extender board in 1A1XA1)	STBY	21.6 ± 4	
9.	1A1A1	1A1XA1-18	1A1UXA-10	Power mode (Insert extender board in 1A1XA1)	STBY	21.6 ± 4	

Table 3-2 . Voltage Measurements - Continued

Item	Component checked	Dvm probe connection		Test set control setting		Dvm indication (volts)	
		LO	HI	Control	Position	Ac	Dc
10.	1A1T1	1A1XA3-2	1A1XA3-4	Power mode (Insert extender board in 1A1XA3)	STBY	232 ± 46	
11.	1A1T1	1A1XA3-2	1A1XA3-8	Power mode (Insert extender board in 1A1XA3)	STBY	232 ± 46	
12.	1A1T1	1A1XA3-4	1A1XA3-8	Power mode (Insert extender board in 1A1XA3)	STBY	232 ± 46	
13.	1A1T1	1A1XA2-14	1A1XA2-16	Power mode (Insert extender board in 1A1XA2)	STBY	11.2 ± 2	
14.	1A1T1	1A1XA2-14	1A1XA2-18	Power mode (Insert extender board in 1A1XA2)	STBY	11.2 ± 2	
15.	1A1T1	1A1XA2-16	1A1XA2-18	Power mode (Insert extender board in 1A1XA2)	STBI	11.2 ± 2	
16.	1A1T1	1A1XA5-16	1A1XA5-8	Power mode (Insert extender board in 1A1XA5)	STBY	11.2 ± 2	

Table 3-2 . Voltage Measurements - Continued

Item	Component checked	Dvm probe connection		Test set control setting		Dvm indication (volts)	
		LO	HI	Control	Position	Ac	Dc
17.	1A1T1	1A1XA5-16	1A1XA5-6	Power mode (Insert extender board in 1A1XA5)	STBY	11.2 ± 2	
18.	1A1T1	1A1XA5-8	1A1XA5-6	Power mode (Insert extender board in 1A1XA5)	STBY	11.2 ± 2	
19.	1A1CR1	1A1TP-6	1A1E12	Power mode	STBY		27 ± 3
20,	1A1CR1	1A1TP-6	1A1E13	Power mode	STBY		27 ± 3
21.	1A1CR2	1A1TP-6	1A1K1-X1	Power mode	STBY		27 ± 3
22.	1A1CR3	1A1K2-X2	1A1K2-X1	Power mode	OPR		27 ± 3
23.	1A1CR4	1A1K3-X	1AK3-X1	Power mode	OPR		27 ± 3
24.	1A1CR5	1A1K4-X2	1A1K4X1	Power mode	OPR		27 ± 3
25.	1A1C1	1A1E1	1A1E18	Power mode	OPR		150 ± 3
26.	1A1CR7	1A1E17	1A1E16	Power mode (Connect jumper wire between 2A1J3 pins H and J. Disconnect jumper wire when test is completed)	OPR		+1.5 ± 1

Table 3-2. Voltage Measurements - Continued

Item	Component checked	Dvm probe connection		Test set control setting		Dvm indication (volts)	
		LO	HI	Control	Position	Ac	Dc
27.	2A1CR1	2A1TB1-13	2A1K1-X1	Power mode	OPR	27 ± 3	
28.	2A1CR2	2A1TB1-13	2A1K2-X1	Power mode	OPR	27 ± 3	
29.	2A1CR3	2A1TB1-13	2A1K3-X1	Power mode	OPR	27 ± 3	
30.	2A1CR4	2A1K4-X2	2A1K4-X1	Power mode PWR SUP TEST	OPR FULL	27 ± 3	
31.	2A1CR5	2A1K5-X2	2A1K5-X1	Power mode PWR SUP TEST	OPR FULL	27 ± 3	
32.	2A1R20	2A1 test point 8	2A1 test point 1	Power mode SLEW	OPR 30 RIGHT	0.75 ± 08	
33.	2A1R20,19	2A1 test point 8	2A1 test point 1	SLEW	20 RIGHT	1.50 ± 0.15	
34.	2A1R20,19,18	2A1 test point 8	2A1 test point 1	SLEW	10 RIGHT	2.25 ± 0.23	
35.	2A1R20.19,18,	2A1 test and 17	2A1 test point 8	SLEW point 1	0 RIGHT	3.00 ± 0.3	
36.	2A1R20,19,18, 17, and 16	2A1 test point 8	2A1 test point 1	SLEW	10 LEFT	3.75 ± 0.38	
37.	2A1R20,19,18, 17,16, and 15	2A1 test point 8	2A1 test point 1	SLEW	20 LEFT	4.50 ± 0.45	
38.	2A1R20,19,18, 17,16,15 and14	2A1 test	2A1 test	SLEW	30 LEFT	5.25 ± 0.53	

Table 3-3. Resistance Measurements

Item	Component checked	Dvm probe connection		Test set control setting		Dvm indication (ohms)
		LO	HI	Control	Position	
1	All relay coils.	X1	X2			290
2	1A1K5	K5-N	K5-A			Greater than 20k
		K5-N	K5-B			Greater than 20k
		K5-N	K5-C			Greater than 20k
3	All diodes	Cathode	Anode			Less than 100
		Anode	Cathode			Greater than 100k
4	Transformer 1A1T1					
	1A1TB1-1	2A1XA14-16				1.8 maximum
	1A1TB1-2	2A1XA14-16				1.8 maximum
	1A1TB1-3	2A1XA14-16				1.8 maximum
	T1-4	T1-5				0.2 maximum
	T1-5	T1-6				0.2 maximum
	T1-4	T1-6				0.2 maximum
	T1-7	T1-8				0.2 maximum
	T1-8	T1-9				0.2 maximum
	T1-7	T1-9				0.2 maximum
	T1-10	T1-11				16.5 maximum
	T1-11	T1-12				16.5 maximum
	T1-10	T1-12				16.5 maximum
	T1-13	T1-14				0.2 maximum
	T1-14	T1-1S				0.2 maximum
	T1-13	T1-15				0.2 maximum
	T1-16	T1-17				0.2 maximum
	T1-17	T1-18				0.2 maximum
	T1-16	T1-18				0.2 maximum

(4) *Continuity checks*. Routine continuity checks between various points in the circuitry can be made using the digital voltmeter of the multimeter and wiring diagrams; however, a list of continuity checks is provided in table 3-4 to ensure a complete continuity check of the circuitry without reference to wiring diagram. The continuity measurements table item column is provided so specific measurements can be easily referenced. The dvm probe connections LO and HI columns specify where the dvm HI probe and LO probe are connected to check the corresponding item continuity measurements. The test unit control setting control and position columns designate test unit control settings which must be made prior to observing the dvm indication for the item circuitry checked. The remarks column contains information of a special nature pertinent to checking continuity for the specific' corresponding item. Continuity is defined as a continuous path with a resistance of less than 2 ohms unless otherwise noted. All measurements are made with power off and circuit breakers open. Prefix all designators with 1A1.

Table 3-4. Continuity Measurements

Item	Dvm probe connection		Test unit control settings		Remarks
	LO	HI	Control	Position	
1	1A1J2-A	1A1A15-E4			
2	1A1J2-B	1AIA15-E6			
3	1A1J2-C	1A1A15-E8			
4	1A1J2-D	1A1A15-E9			
5	1A1J1-A	1A1A15-E2			
6	1A1J1-B	1A1A15-E3			
7	1A1K1-D2	1A1DS2-3	Power mode sw1tch 1A1S1	STBY, OPR, and RESET	
8	1A1K1-D1	1A1K2-X1	1A1S1	OPR	
9	1A1K1-D2	1A1XA6-9	1A1S1	OPR	
10	1A1TP-6	1A1J6-1	VIDEO/SIM TEST	SIM TEST	
11	1A1TP6	1A1XA8-16	SIM TEST		
12	1A1XA9-1	JA1XA9-21	FIELD OF VIEW 1A1S3	1/2	
13	1A1XA9-1	1A1XA9-18 and -21	1A1S3	FULL	
14	1A1J6-AA	11ATP-2			
15	1A1TP-2	1A1S3A-C4	SLEW 1A1S5	30° LEFT	
16	1A1TP-2	1A1S3B-C1	1A1S5	20° LEFT	
17	1A1TP-2	1A1S3B-G2	1A1S5	10° LEFT	
18	1A1TP-2	1A1S3B-C3	1A1S5	0°	
19	1A1TP-2	1A1S3B-C4	1A1S5	10° RIGHT	
20	1A1TP-2	1A1S3C-C1	1A1S5	20° RIGHT	
21	1A1TP-2	1A-S3C-C2	1A1S5	30° RIGHT	
22	1A1S3A-C4	1A1XA10-16	1A1S3	1/4	
23	1A1S3A-C4	1A1XA10-10 1A 1S2B-1 and -2	1A1S3	1/2	
24	1A1S3A-C4	1A1S3B-3, 6, 7, 8, 9, and 12 1A1S3C-3 and -6 1A1XA10-11	1A1S3	FULL	
25	1A1S3B-C1	1A1XA10-10	1A1S3	1/4	
26	1A1S3B-C1	1A1XA10-11	1A1S3	FULL	
27	1A1S3B-C2	1A1XA10-4 1A1S3B-5	1A1S3	1/4	
28	1A1S3B-C2	1A1XA10-11	1A1S3	FULL	
29	1A1S3B-C3	1A1XA10-11			
30	1A1S3B-C4	1A1XA10-5 1A1S3B-11	1A1S3	1/4	
31	1A1S3B-C4	1A1XA10-11	1A1S3	FULL	

Table 3-4. Continuity Measurements-Continued

Item	Dvm probe connection		Test unit control settings		Remarks
	LO	HI	Control	Position	
32	1A1S3C-C1	1A1XA10-9	1A1S3	1/4	
		1A1S3C-2			
		and 5			
33	1A1S3C-C2	1A1XA10-7	1A1S3	1/4	
34	1A1S3C-C2	1A1XA10-9	1A1S3	1/2	
35	1A1S3C-C2	1A1XA10-11	1A1S3	FULL	
36	1A1E1	1A1TP-10	V/H 1A1S4	OFF	
37	1A1XA9-2	1A1A7-g	1A1S4	ON	
38	1A1E1	1A1XA10-23	HOT SPOT 1A1S6	OFF	
39	1A1XA9-23	1A1XA10-23	1A1S6	ON	
40	1A1test point 6	1A1J6-k	1A1S6	ON	
41	1A1test point 6	2A1K4-X2	PWR SUP TEST		
			1A1S7	FULL	
42	1A1J5-A	2A1K5-X1	1A1S8	FULL	
43	1A1SUP VOLT	2A1K5-C2	SUPPLY VOLTAGE		
			1A1S8	250V	
		1A1J4-(TGG			
44	1A1SUP VOLT	2A1K5-B2	1A1S8	150V	
		1A1J4-FF			
45	1A1SUP VOLT	1A1TP-7	1A1S8	6.3V	
		2A1K4-A2			
		1A1J4-K			
46	1A1SUP VOLT	12A1K4-C2	1A1S8	5V	
		1A1J4-CC			
47	1A1SUP VOLT	2A1K4-D2	1A1SS	+15V	
		1A1J4-EE			
48	1A1SUP VOLT	2A1K5-A2	1A1S8	-15V	
		1A1J4-DD			
49	1A1VERT SWP	1A1J8-H	VERT SWP 1A1S9	CLK PULSE	
50	1A1VERT SWP	1A1J8-N	1A1S9	WRT SWP V	
51	1A1VERT SWP	1A1XA11-6	1A1S9	COM.XP SWP V	
52	1A1VERT SWP	1A1XA11-20	1A1S9	TDI SYNC	
53	1A1VERT SWP	1A1J6-V	1A1S9	RD SYNC	
54	1A1VERT SWP	1A1XA11-3	1A1S9	RD SWP V	
55	1A1HORIZ SWP	1A1J8-E	HORIZ SWP 1A1S10	100 KHZ OSC	
56	1AIHORIZ SWP	1A1J8-G	1A1S10	WRT SWP GEN	
57	1A1HORIZ SWP	1A1XA11-14	1A1S10	WRT SWP	
58	1A1HORIZ SWP	1A1XA11-10	1A1S10	RD HORIZ SYNC	
59	1A1CRT	1A1XA9-8	COUNTER 1A1S11	VID GATE	
		2A1J3-z			
60	1A1CRT	1A1J8-H	1A1S11	V/H CLK PULSE	
61	1A1CRT	1A1J8J	1A1S11	BLANK PULSE	
62	1A1CRT	2A1XA1-23	1A1S11	100 KHZ OSC	
63	1A1test point 6	1A1J6-q	VIDEO 1A1S12	VID A	
64	1A1test point 6	1A1XA8-16			
		1A1J6-n	1AS12	VID B	
65	LRU A	1A1XA11-17	LRU 1A1S13	01	
66	LRU A	1A1J8-T	1A1S13	02	
67	LRU A	1A1XA12-16	1A1S13	03	
68	LRU A	1A1XA12-8	1A1S13	04	
69	LRU A	1A1J8-R	1A1S13	05	
70	LRU B	1A1XA12-17	1A1S13	01	
71	LRU B	1A1XA12-6	1A1S13	02	
72	LRU B	1A1XA11-8	1A1S13	03	
73	LRU E	1A1J8-L	1A1S13	04	
74	Test point 1	1A11J7-D	1A1S13	03	
75	1A1J25 TP-1	1A1J7-C	1A1S13	04	
76	1A1J25 TP-1	1A1J7-B	1A1S13	05	
77	1A1E1	1A1J6-s	1A1S13	03	
78	1A1E1	1A1J6-t	1A1S13	04	
79	1A1E1	1A1J4-p	1A1S13	05	
80	VID 1	1A1XA-8			
		1A1J7-Y			

Table 3-4. Continuity Measurements-Continued

Item	Dvm probe connection		Test unit control settings		Remarks
	LO	HI	Control	Position	
81	VID 2	1A1XA8-5 1A1J7-a			
82	TEST 1	1A1XA11-16			
83	TEST 2	1A1XA11-1			
84	TEST 3	1A1XA9-7 2A1XA4-16 1A1XA5-17 2A1XA9-18 2A1XA1-3			
85	TEST 4	1A1XA7-1 1A1XA8-15			
86	TEST 5	1A1XA10-8 1A1J7-N 1A1XA9-5			
87	TEST 6	1A1XA9-9			
88	TEST' 7	1A1A8-1 2A1A6-16			
89	TEST 8	1A1A8-9 1A1A6-18			
9"	Test point 3	1A1K3-C1 2A1K2-A2			
o]	Test point 4	1A1K3-D1 2A1K2-B2			
9'	Test point 5	1A1J6-K			
93	Test point 6	1A1TB1-7			
94	Test point 11	1A1J4-E			
95	Test point 12	1A1E1			
96	VERT SWP	XA9-7 2A1J3-w	VERT SWEEP 2A1S1	WRT COMP SWP V	
9.	VERT SWP	2A1J4-G	2A1S1	WRT DEFL CUR	
98	VERT SWP	2A1J4-H	2A1S1	RD DEFL CUR	
99	VERT SWP	2A1XA3-6 2A1J3-y	2A1S1	RD SWP V	
100	VIDEO	2A1J2-c	VIDEO 2A1S2	WRT VID	
101	VIDEO	2AIXA13-11 2AIJ2-e	2A1S2	RD VID	
102	VIDEO	2A1XA6-11 1A1XA8-11	2A1S2	INT MOD	
103	VIDEO	2A1J4-i 2A1XA6-14	2A1S2 INPUTS 2A1S8	HS MOD 01 through 06	
104	HORIZ SWP	2A1J3-x 2A1XA,5-4	HORIZ SWEEP 2A1S3	WRT SWP	
105	HORIZ SWP	2A1J4-F	2A1S3	WRT DEFL CUR	
106	HORIZ SWP	2AIJ4-Y 2A1XA2-6	2A1S3	RD HORIZ SYNC	
107	Test point 6	2A1R3-2 2A1R2-2 2A1J3-Z, W, f, and c.			
107A	HORIZ SWP	2A1J2-g and 2A1E22	2A1S3	RD DEFL CUR	
108	HORIZ SWP	2A1XA8-6	2A1S3	SKEW CORR	
109	SUP VOLT	2A1J4J	SUPPLY VOLTAGE 2A1S4	1 KV	
110	SUP VOLT	2A1J4-K	2A1S4	4.4 KV (LC)	
111	SUP VOLT	2A1J4-L	2A1S4	4.4 KV (HC)	
112	SUP VOLT	1A1K4-B1 2A1K3-C2	2A1S4	250 V	
113	SUP VOLT	1A1K4-A1 2A1K3-W2 2ALP1-9 2A1XA12-16 2A1R23-2	2A1S4	150 V	

Table 3-4. Continuity Measurements-Continued

Item	Dvm probe connection		Test unit control settings		Remarks
	LO	HI	Control	Position	
114	SUP VOLT	1A1K3-A1 1A1XA9-9 1A1XA10-21 1A1XA7-22 1A1XA7-F 2A1K2-C2 2A1XA8-21 2A1XA1-16	2A1S4	5 V	
115	SUP VOLT	1A1K4-C1 1A1XA9-23 1A1XA8-23 1A1S6-6 1A1XA7-2 2A1K2-D2 2A1XA12-8 2A1XA13-17 2A1XA6-23 2A1XA1-22 2A1XA2-23 2A1XA3-23 2A1XA4-23 2A1XA5-23 2A1XA7-23 2A1XA10-23 2A1XA8-23 2A 1XA9-23 2A 1XA11-23 2A1J3-g,a, d, X 2A1S5-1 2A1S11-3	2A1S4	+15 V	
116	SUP VOLT	1A1K3-B1 1A1XA9-1 1A1XA8S-22 1A1XA10-22 2A1K3-A2 2A1XA12-21 2A1XA13-10 2A1XA6-22 2A1XA1-18 2A1XA4-22 2A1XA3-2 2A1XA5-22 2A1XA7-22 2A1XA8-22 2A1XA10-22 2A1XA9-22 2A1XA11-22 2A1S6A-C1, C2 2A1J3-Z, W, f, c 2A1S11-6 2A 1R2-2 2A1R3-2	2A1S4	-15 V	
117	2A1E1	1A1J4-r 2A1XA7-7	TUBE PROTECT/ FRAME HOLD 2A1S5	TUBE PROTECT	
118	2A1E1	2A1XA13-18 2A1J3-p	2A1S5	TUBE PROTECT	
119	1A1J4-r	2A1J3-a	2A1S5	FRAME HOLD	
120	2A1E1	2A1XA1-14	2A1S5	FRAME HOLD	
121	2A1S6A-C2	2A1XA5-11	FIELD OF VIEW 2A1S6	1/2	
122	2A1S6A-C2 2A1S6A-C1	2A1XA5-11 2A1XA5-15	2A1S6 2A1S6	FULL FULL	

Table 3-4. Continuity Measurements-Continued

Item	Dvm probe connection		Test unit control settings		Remarks
	LO	HI	Control	Position	
123	2A1R1-2	2A1XA13-8	2A1S6	1/4	
		2A1J2-f			
124	2A1R1-2	2A1XA13-7	2A1S6	1/2	
		2A1J2-d			
125	2A1R1-2	2A1XA13-6	2A1S6	FULL	
		2A1J2-b			
126	2A1S6A-C4	Test point 2	FIELD OF VIEW	1/4	
127	Test point 1	2A1S6A-C4	SLEW 2A1S7	30 LEFT	
128	Test point 1	2A1S6B-C1	2A1S7	20 LEFT	
129	Test point 1	2A1S6B-C2	2A1S7	10 LEFT	
130	Test point 1	2A1XA5-16	2A1S7	0	
131	Test point 1	2A1XS6-C4	2A1S7	10 RIGHT	
132	Test point 1	2A1S6C-C1	2A1S7	20 RIGHT	
133	Test point 1	2B1S6C-C2	2A1S7	30 RIGHT	
134	2A1S6A-C4	2A1E9	2A1S6	1/2	
		2A1S6B-A1 and A2			
135	2A1S6A-C4	2A1E15	2A1S6	FULL	
		2A1S6B-C3 6,7,8,			
		9, and 12			
		2A 1S6C-3 and 6			
136	2A1S6B-C1	2A1E10	2A1S6	1/4	
137	2A1S6B-C1	2A1E12	2A1S6	FULL	
138	2A1S6B-C2	2A1E11	2A1S6	1/4	
		2A1S6B-5			
139	2A1S6B-C2	2A1E15	2A1S6	FULL	
140	2A1S6B-C3	2ALE15			
141	2A1S6B-C4	2A1E14	2A1S6	1/4	
		2A166B-11			
142	2A1S6B-C4	2A1E15	2A1S6	FULL	
143	2A1S6C-C1	2A1E17	2A1S6	1/4	
		2A1S6C-2 and 5			
144	2AS6C-	2A1S6C-C 2A1E12	2A1S6	FULL	
145	2A1S6C-C2	2A1E16	2A1S6	1/4	
146	2A1S6C-C2	2A1E17	2A1S6	1/2	
147	2A1S6C-C2	2A1E12	2A1S6	FULL	
148	INPUT A	2A1XA9-6	INPUTS 2A1S8	02	
149	INPUT A	2A1XA10-7	2A1S8	03	
150	INPUT A	2A1XA11-4	2A1S8	04	
151	INPUT A	2A1XA6-6	2A1S8	05 or 06	
152	INPUT B	2A1XA1-1	2A1S8		
		2A 1S8B-8			
		2A 1J4-i		07 or 08	
153	INPUT C	2A 1J4-g	2A1S8	01	
		2A1XA5-8			
154	INPUT C	2A1XA7-14	2A1S8	02	
155	INPUT C	2A1XA7-4	2A1S8	03	
156	INPUT C	2A1XA4-8	2A1S8	04	
157	INPUT C	2A1XA7-6	2A1S8	05	
		2A1XA2-3			
158	INPUT D	2A1XA1-2	2A1S8	07	
		2A1TB1-12	2A1S8	07	
159	Test point 4	2A1J2-R	2A1S8	05	
160	Test point 4	2A1XA6-7	2A1S8	06	
161	LRU A	2A1J4-M	LRU 2A1S9	01	
162	LRU A	2A1J4-N	2A1S9	02	
163	LRU A	2A1J4-P	2A1S9	03	
164	LRU A	2A1J4-R	2A1S9	04	
165	LRU A	2A1J4-S	2A1S9	05	
166	LRU A	2A1J4-T	2A1S9	06	
167	LRU B	2A1J4-B	2A1S9	01	
168	LRU B	2A1J4-C	2A1S9	02	

Table 3-4. Continuity Measurements-Continued

Item	Dvm probe connection		Test unit control settings		Remarks
	LO	HI	Control	Position	
169	LRU E	2A1J4-D	2A1S9	03	
170	LRU B	2A1J4-E	2A1S9	04	
171	LRU C	2A1XA13-23	2A1S9	01	
172	LRU C	2AIXA13-2	2A1S9	02	
173	LRU C	2A1XA13-1	2A1S9	03	
174	LFIU C	2A1XA13-3	2A1S9	04	
175	2A1J4-U	2A1S10A-5 2A1S10B-4 and 7 2A1P1-15 2A1J25 2A1XA12-22	ALIGNMENT 2A1S10	01	
176	2A1J4-U	2A1S1OA-7 2AIS1OB-2 and 5 2A1E1	2A1S10	01	
177	2A1J4-V	2A1E1	2A1S10	01	
178	2A1J4-V	2A1S1OB-7	2A1S10	03	
179	2A1J4-W	2A1S1OC-2, 3 and 4 2A1S1OD-5, 6 and 7 Test point 4 2A1S8E-C	2A1S10	01	
180	2A1J4-X	Test point 4	2A1S10	04	
181	2A1J3-E	2A1XA13-22	2A1S10	OFF	
182	2A1J3-E	1A1K2-D1 1A1DS3-2 1A1K3-X1 1A1K4-X1 1A1XA8-17 1A1S7-2 1A1J5-A 2A1J3-J 2A1K1-A2 2A1XA6-8 2A1XA13-20 2A1S10E-C2, 3, 4, 5, 6, and 7	2A1S10	01	
183	2A1J3-j	2A1J3-n 2A1J3-g	RD TEST 2A1S11	NOM	
184	2A1J3-v	2A1XA2-1 2A1XA3-18 2A1XA12-2	VERT TEST 2A1S12	NOM	
185	2A1J3-v	2A1XA12-3	2A1S12	TEST	
186	2A1J27	2A1TB1-2			
187	2A1J28	2A1TB1-11			
188	2A1J30	2A1E1			
189	1A1J3-n	1A1J4-BB			
190	1A1J6-X	1A1XA11-21			
191	1A1J6-U	1A1XA12-7			
192	1A1J6-J	1A1J4-H			
193	1A1JS-Y	1A1XA11-11			
194	1A1J8-a	1A1XA11-2			
195	1A1J8-e	1A1XA11-19			
196	1A1J8-g	1A1XA11-9			
197	1A1J8-i	1A1XA11-18			
198	1A1J4-w	1A1XA11-7			
199	1A1J4-X	1A1XA11-15			
200	1A1J4-y	1A1XA11-5			
201	1A1J4-U	1A1XA12-10			
202	1A1J4-v	1A1XA12-18			
203	1A1J4-z	1A1XA12-14			
204	1A1K1-C1	2A1K1-D2			
205	1A1K1-B1	2A1K1-C2			
206	1A1K1-A1	2A1K1-B2			

Table 3-4. Continuity Measurements - Continued

Item	Dvm probe connection		Test unit control settings		Remarks
	LO	HI	Control	Position	
207	1A1T1-4	2A1XA14-16			
208	1A1T1-5	2A1XA14-10			
209	1A1T1-6	2A1XA14-18			
210	1A1K2-A1	1A1J5J			
211	1A1K2-B1	1A1J5-K			
212	1ALK2-C1	1A1J5-L			
213	1A1K2-D1	1A1J5-A			
214	A1J5-M	1A1A15E9			
215	1A1J5-B	1A15A1E3			
216	2A1J2-U	2A1R2-3			
217	2A1J2-F	2A1R2-1 2A1R3-1 2A1J2-M 2A1E1 2A1E21			
218	2A1J2-W	2A1R3-			
219	2A1J2-L	2A1XA1-17			
220	2A1J2-Z	2A1R1-1			

(5) *Intermittent troubles*. When troubleshooting, the possibility of intermittent troubles should not be overlooked. This trouble can often be made to appear by tapping or jarring the equipment. Check wiring and connections.

3-6. Interunit Troubleshooting

a. Defective Signal Monitoring. Failure to monitor a selected voltage or signal may be caused by defective external test equipment. If an operational check fails to sectionalize trouble to a defective unit or a defective major functional area, follow the procedures given in (1), (2), and (3) below.

(1) *External test equipment check*. All external test equipment should function properly. Perform operational checks on each unit of external test equipment as described in the applicable test equipment manual.

(2) *Control units check*. All major functional areas of the control units should function properly, including the active circuits (semiconductor circuits) and the controls.

(a) Active circuits. If any of the transistor or diode circuits are suspected of causing a malfunction, isolated the trouble by using voltage and resistance measurements with external test equipment.

(b) Controls. To verify that all controls are functioning properly, perform continuity measurements (table 3-4) while the controls are rotated through each position.

(3) *Connectors check*. The continuity measurements will aid in determining whether a connector is contributing to the malfunction.

b. Checking Cable Assemblies. All interconnecting cable assemblies should be checked for signs of insulation deterioration and for operas or shorts near the connectors. Check connectors for bent or deformed pins and for signs of arcing.

Section III. REMOVAL AND REPLACEMENT

3-7. Removal

All parts may be removed using standard tools and maintenance procedures.

a. The control units are removed by disengaging the screws along the edge of the panels and sliding the chassis from the cases. Refer to parts location diagram, figures 3-3 and 3-4 when removing parts and subassemblies.

b. Access to printed circuit boards is gained by removing the 5 screws securing the hinged cover and swinging it open.

c. To gain access to the remaining chassis mounted components, remove the 6 screws securing the two hinged portions of the chassis and swinging it open.

NOTE

Exercise care when opening the hinged portion of the chassis. The shifting center of gravity can cause the unit to fall, damaging the chassis or components.

d. Access to the filter assembly is gained by removing the two retaining nuts securing 1A1J1 and 1A1J2 to the panel and removing the 8 panhead screws securing the filter assembly case to the control unit panel. Refer to parts location diagram, figure 3-5, when removing parts and subassemblies.

3-8. Replacement

All parts may be replaced using standard tools and maintenance procedures. Refer to part location diagrams when removing parts and subassemblies.

a. The control unit is replaced by sliding the chassis back into the case and securing the screws along the edge of the panel.

b. Secure the printed circuit board hinged cover with the five screws.

c. Secure the hinged portion of the chassis with the six screws.

d. To replace the filter assembly, secure 1A1J1 and 1A1J2 to the control unit panel with the two retaining nuts; secure the filter assembly case to the control unit panel with the eight panhead screws. Refer to the parts location diagram, figure 3-5, when replacing parts and subassemblies.

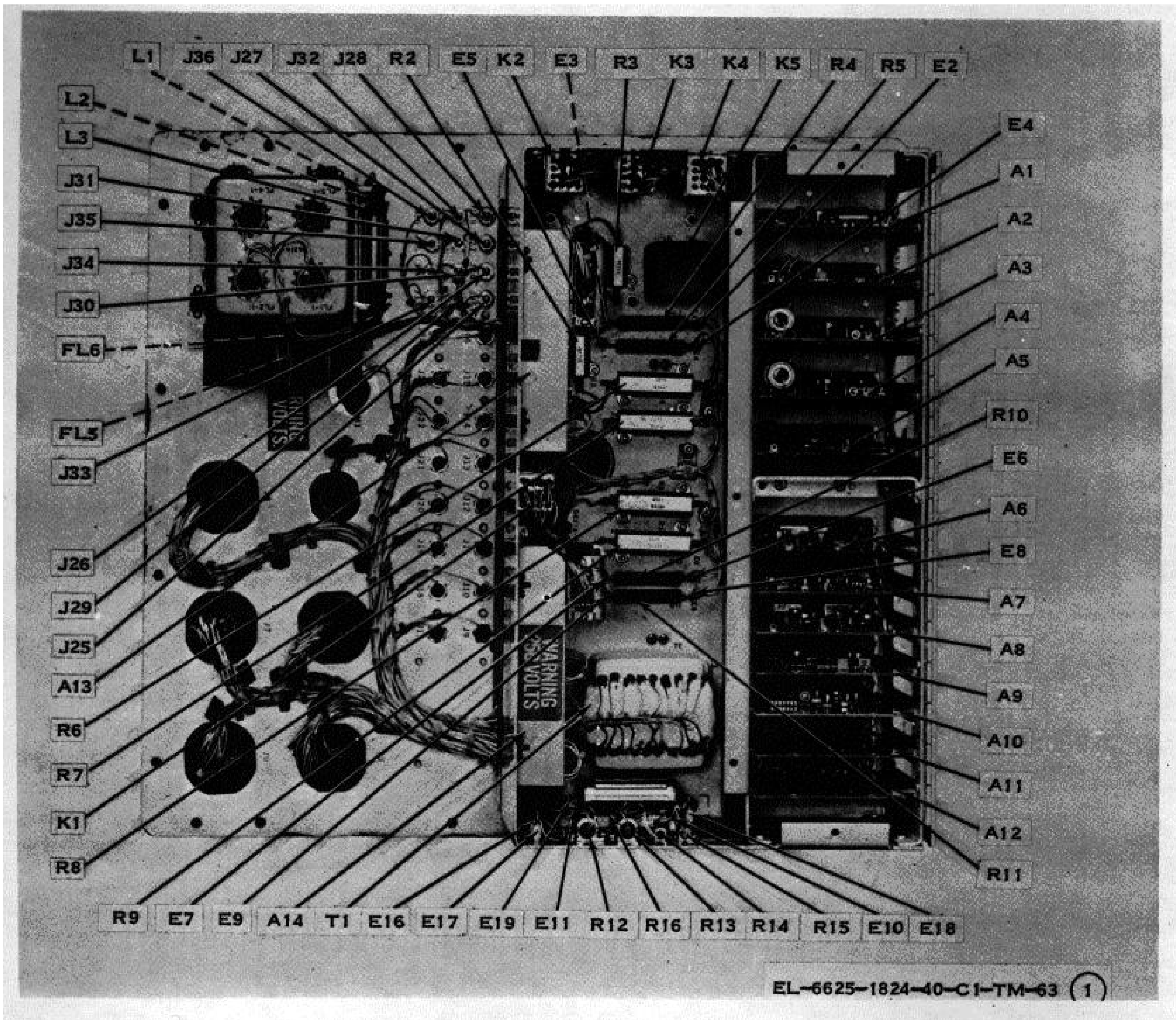


Figure 3-3(1). Parts location, control unit 1A1 (part 1 of 2)

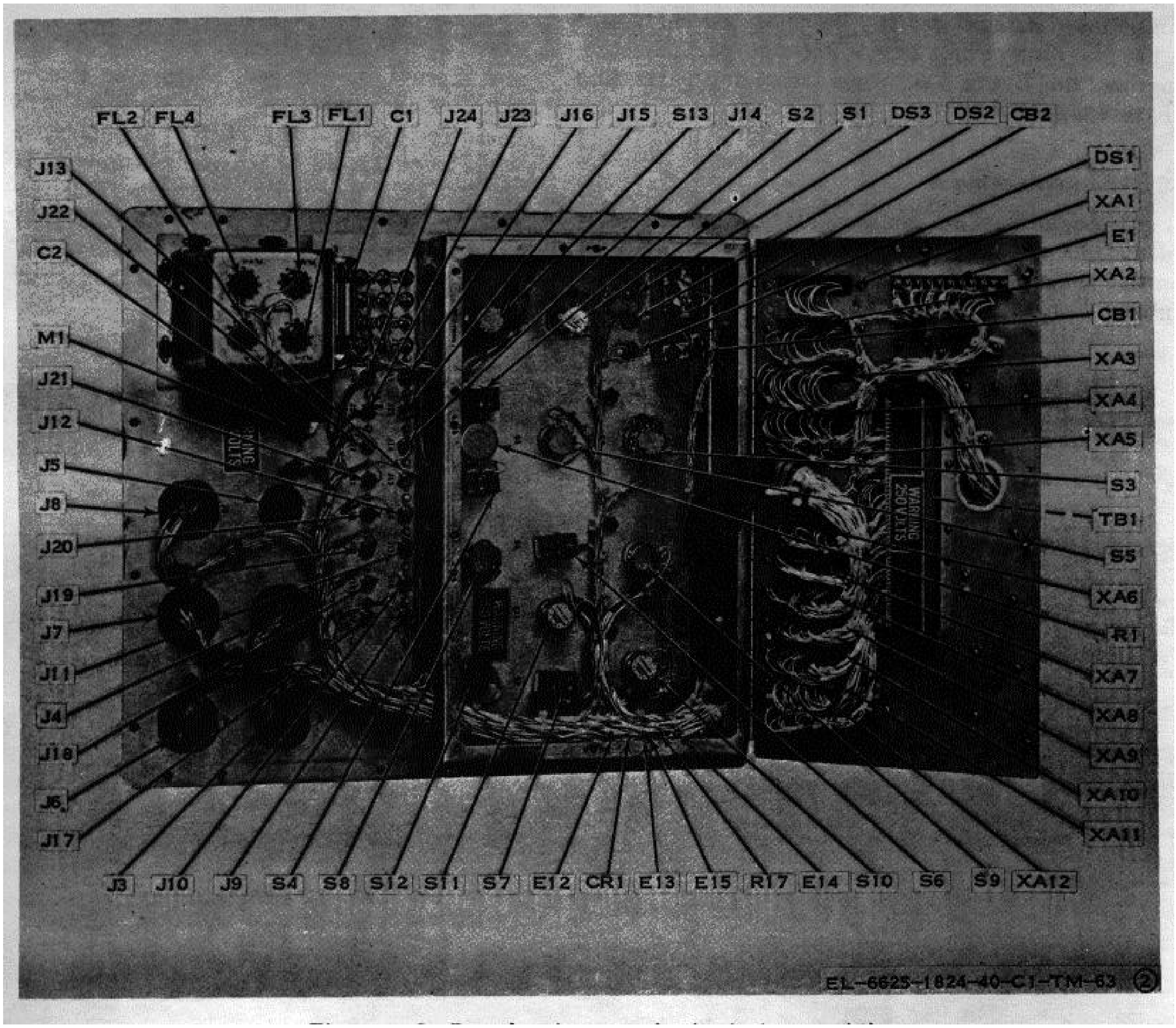


Figure 3-3(2). Parts location, control unit 1A1 (part 2 of 2)

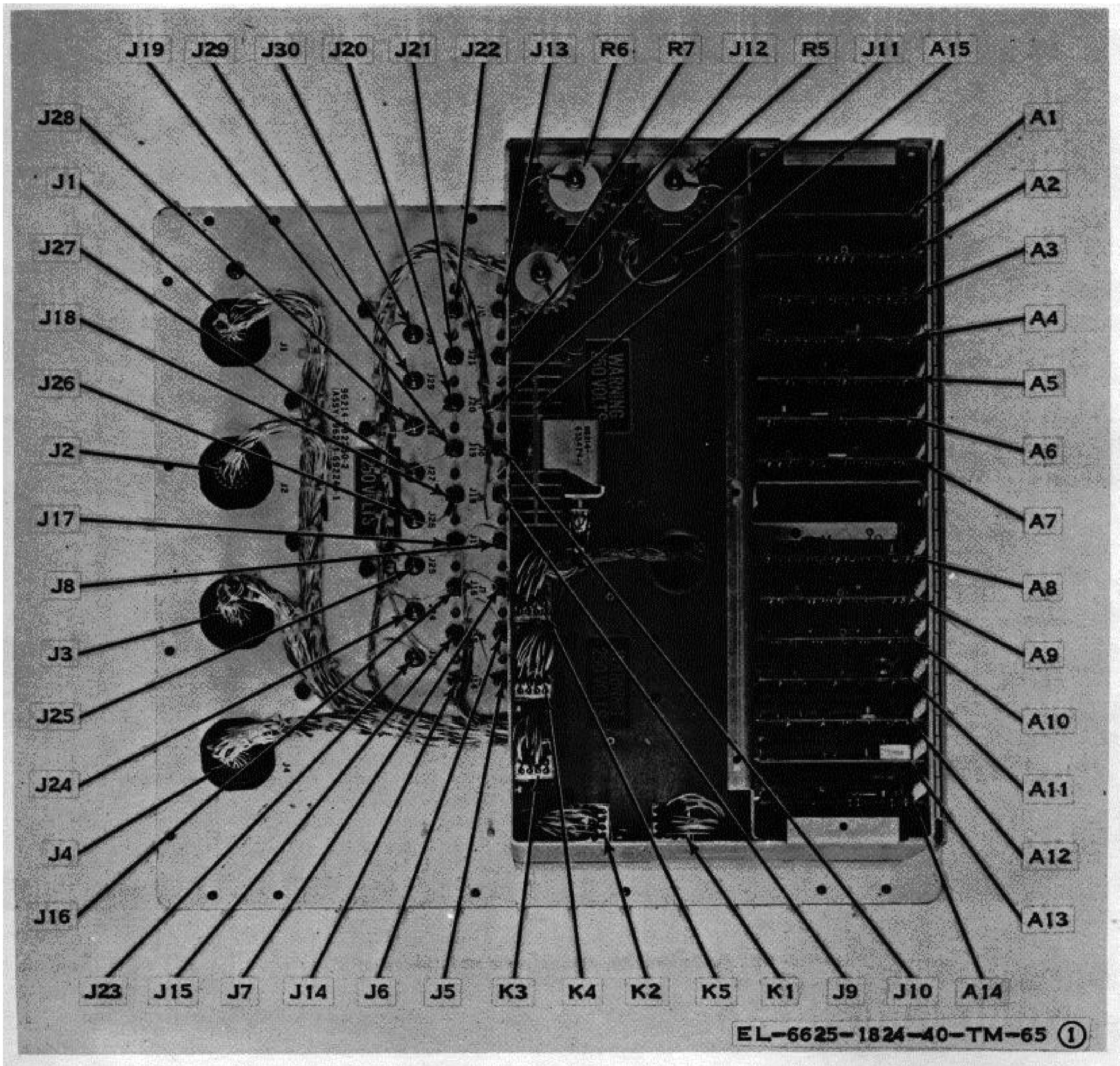


Figure 3-4(1). Parts location, control unit 2A1 (part 1 of 2)

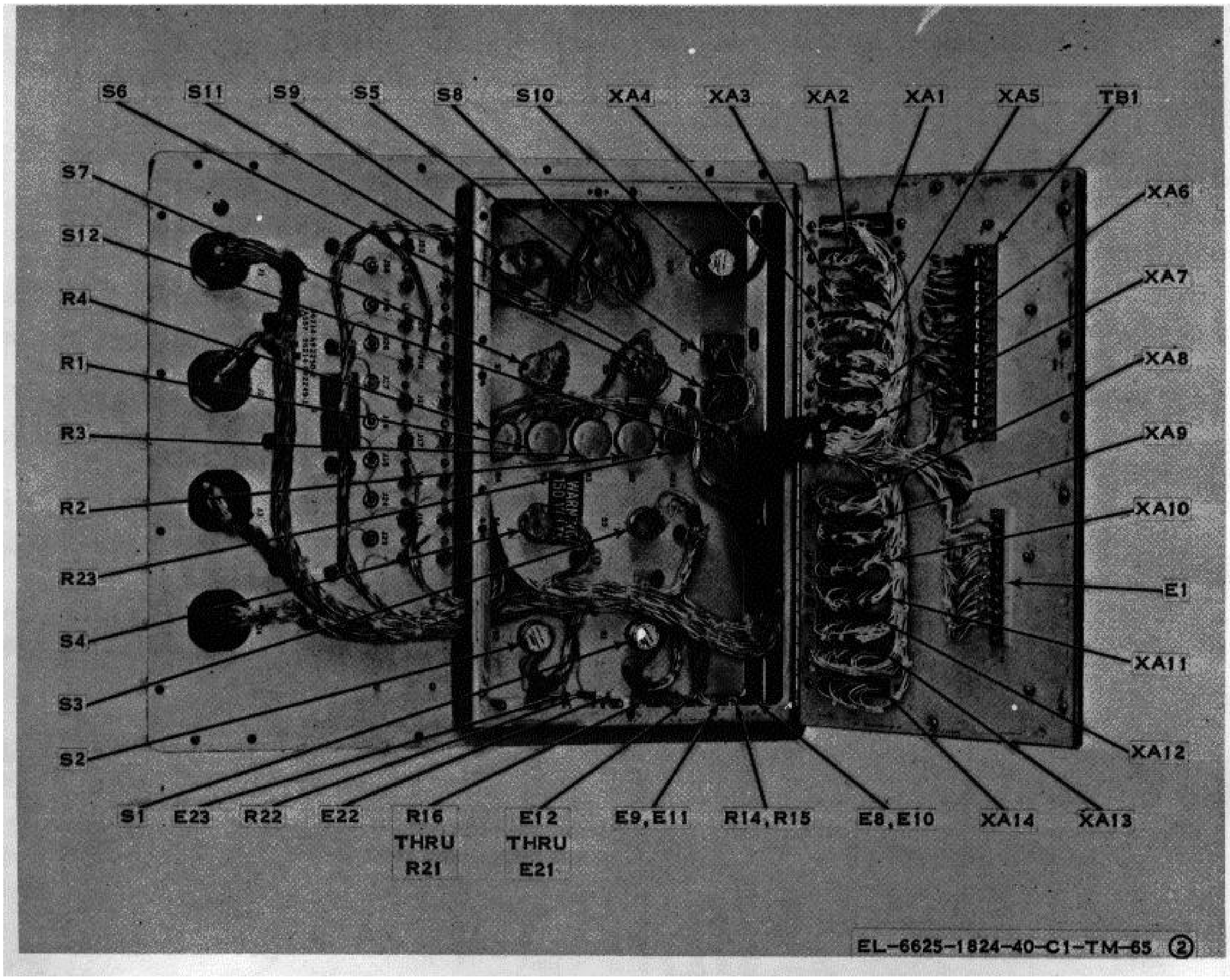


Figure 3-4(2). Parts location, control unit 2A1 (part 2 of 2)

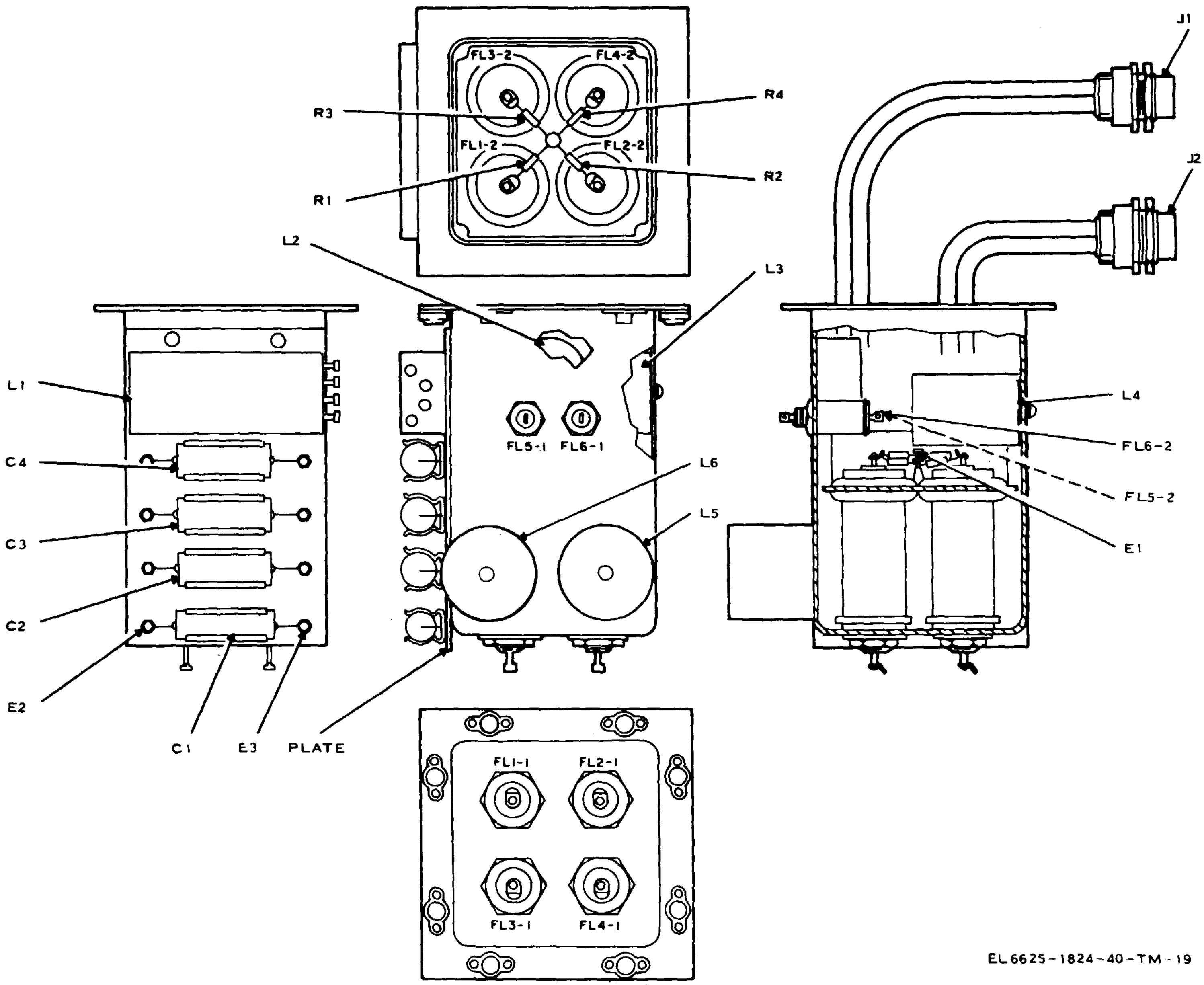


Figure 3-5. Parts location, filter assembly 1A1A15.

Section IV. ADJUSTMENT AND ALIGNMENT

3-9. Adjustment Procedure

a. Initial Preparation.

(1) Perform the removal procedure (para 3-7)to remove control units 1Al&1A2from the carrying cases and gain access to the printed circuit boards.

(2) Use extender boards obtained from the electronic maintenance kit as necessary for gaining access to the board test points and the variable resistors.

(3) Perform the starting procedures as outlined in TM 11-6625-1824-12.

(4) Remove power from the converter test set when removing or replacing printed circuit boards.

(5) Perform the preparation for use procedures for the test equipment as outlined in paragraph 33.

WARNING

DEATH or SERIOUS INJURY may result from contact with 115-VAC, 400-Hz, 3-PHASE power existing within this equipment.

b. Test Equipment.

(1) Oscilloscope AN/USM-281A.

(2) Digital Voltmeter, Non-Linear Systems Model X-2.

c. Adjustments.

(1) Locate -15-vdc power supply board 1A1A1 (fig. 3-3 (1)).

(2) Set SUPPLY VOLTAGE 2A1S4 to -15V.

(3) Connect the dvm LO probe to the converter test set.

(4) Connect the dvm HI probe to test point SUP VOLT, 2A1J8.

(5) Adjust 1A1A1R12 for -15 ± 0.02 vdc.

(6) Set SUPPLY VOLTAGE 2A1S4 to 5V.

(7) Locate integrated circuit power supply 1A1A2 (fig. 3-3 (1)).

(8) Adjust 1A1A2R14 for + 5 ± 0.05 vdc.

(9) Set SUPPLY VOLTAGE 2A1S4 to 250V.

(10) Locate 150/250-vdc power supply 1A1A3 (fig. 3-3 (1)).

(11) Adjust 1A1A3R20 for 250 ± 1.0 vdc.

(12) Set SUPPLY VOLTAGE 2A1S4 to 15OV.

(13) Locate 150/250-vdc power supply 1A1A4 (fig. 3-3 (1)).

(14) Adjust 1AlA4R20 for 150 ±1.0 vdc.

(15) Set SUPPLY VOLTAGE 2A1S4 to 15V.

(16) Locate 15-vdc power supply 2A1A14 (fig. 3-4 (1)).

(17) Adjust 2A1A14R12 for 15 ±0.02 vdc.

(18) Connect the dvm LO probe to test point 4 on 1A1.

(19) Connect the dvm HI probe to test point 3 on 1A1.

(20) Locate storage tube filament power supply 1A1A5 (fig. 3-3 (1)).

(21) Adjust 1A1A5R9 for 6.3 ±0.5 vdc.

(22) Connect the dvm LO probe to test point 12 on 1A1.

(23) Locate power control board 1A1A6 (fig. 3-3 (1)).

(24) Connect the dvm HI probe to 1A1A6-J2 (red).

(25) Adjust 1A1A6R21 for 3.2 ±0.1 vdc.

(26) Move the dvm HI probe to 1A1A6J3 (orange).

(27) Adjust 1AIA6R19 for 2.3 ±0.1 vdc.

(28) Locate -15-vdc power supply 1A1A1 (fig. 33 (1)).

(29) Move the dvm HI probe to 1A1AJ3 (orange).

(30) Adjust 1A1A1R12 for -15.9 ±0.02 vdc.

(31) Adjust 1A1A6R21 cw until FAIL lamp A1DS1 lights, then cow one half turn.

(32) Adjust 1A1A1R12 for -14.1 ± 0.02 vdc. Verify FALL lamp 1A1DS1 extinguishes after RESET then back to OPR.

(33) Adjust 1A1A6R19 ccw until FALL lamp 11DS1 lights.

(34) Adjust 1A1A6R19 cw one-half turn (180°).

(35) Adjust 1A1AR12 for -15 ±0.02 vdc. Verify FALL lamp 1A1DS1 extinguishes after REST then back to OPR.

(36) Remove the dvm probes.

(37) Connect the scope to test point TEST 4; observe waveform C, figure 3-2.

(38) Locate CS--VC simulator 1A1A7 (fig. 33 (1)).

(39) Adjust 1A1A7R6 for period of 25 ±3 μsec.

(40) Adjust 1A1A7R17 for amplitude of 1.2 ± 0.1 volt.

(41) Set HORIZ SWEEP 2A1S3 to RD HORIZ SYNC.

(42) Move the scope CH 2 probe to test point HORIZ SWP 2A1J6.

(43) Locate sync generator 2A1A2 (fig. 3-4 (1)).

(44) Connect the scope CH 1 probe to 2A1A2J1 (white). Observe waveform AJ, figure 3-2.

(45) Adjust 2A1A2R12 for a 0.5 ± 0.05 μsec time difference between the trailing edges of the waveforms.

(46) Set VERT SWEEP 2A1S1 to RD SWP V.

(47) Connect the scope to test point VERT SWP. Observe waveform M, figure 3-2.

(48) Locate read vertical sweep generator 2A1A3 (fig. 3-4 (1)).

(49) Adjust 2A1A3R17 for 12 ± 0.4 volts peak-to-peak.

(50) Adjust 2A1A3R23 to center waveform about zero, DC level.

(51) Move the scope probe to test point INPUT C Set INPUT switch to 02 and observe waveform AK, figure 3-2.

(52) Locate v/h clock pulse generator 2A1A7 (fig. 3-4 (1)).

(53) Adjust 2A1A7R2 for a period compatible with FIELD OF VIEW 1A1S6 settings as follows: FULL2.46 ± 0.40 msec; 1/2-1.23 ± 0.20 msec; 1/4-0.62 ± 0.10 msec.

(54) Reset all the switches on 1A1 and 1A2 to the ccw position except for the power mode switch 1AlSI and INPUT switch 2A1S8.

(55) Locate, write vertical. sweep generator 2A1A8 (fig. 3-4 (1)).

(56) Connect a scope to 2A1ASJ2 (red). Observe waveform AF, figure 3-2.

(57) Adjust 2A1A8R10 for 0 ± 200 mv at beginning of ramp.

(58) Adjust 2A1A8R2 for 5 ± 0.15 volts amplitude.

(59) Set VERT SWEEP 2A1S1 to WRT COMP SWP V.

(60) Connect the scope to test point VERT SWP 2A1J1. Observe waveform T, figure 3-2.

(61) Locate erase vertical sweep generator 2A1A9 (fig. 3-4 (1)).

(62) Adjust 2A1A9R4 for a negative value of -5.0 ± 0.05 volts.

(63) Adjust 2A1A9R18 for a positive value of 60 ± 30 mv.

NOTE

Due to the slow period (2.5 sec) the waveform cannot be seen in its entirety. To measure the positive and negative easily, set scope to AC.

(64) Connect TRIG IN to converter test set unit 1 TEST 3 and set scope to EXT TRIG.

(65) Set FIELD OF VIEW 2A1S6 to FULL. Set SLEW 2A1S7 to 0°. Set HORIZ SWEEP 2A1S3 to WRT SWP.

(66) Connect the scope to HORIZ swp ZA1J6. Observe waveform N, figure 3-2.

(67) Locate write horizontal slew and fov adder 2A1A5 (fig. 3-4 (1)).

(68) Note where the positive going slope crosses the slope zero reference. Change FIELD OF VIEW 2A1S6 to 1/2 and 1/4. Adjust 2A1A5R36 until all three slopes cross the zero reference within ± 2 20 µsec of each other.

(69) Return FIELD OF VIEW 2A1S6 to FULL.

(70) Locate write horizontal sweep generator 2A1A4.

(71) Adjust 2A1A4R42 for -4.5 ± 0.1-volt peak.

(72) Adjust 2A1A4R28 for +4.5 ± 0.1-volt peak.

(73) Adjust 2A1A4R7 for 350 ± 75 µsec positive steady state tine.

(74) Adjust 2A1A4R30 for 350 ± 75 µsec negative steady state time.

(75) Set INPUTS 2A1S8 to 01.

(76) Connect the scope to test point INPUJT C. Observe waveform R, figure 3-2.

(77) Adjust 2A1A5R14 for 35.0 ± 7.5 µsec for the first pulsewidth.

(78) Adjust 2A1A.,R17 for 350 ± 75 µsec for the second pulsewidth.

(79) Set FIELD 0 VIEJ -switch on 1A1 to 1/2. Connect the scope to 2A1J4-c. Observe waveform on scope. If waveform is not present on 1/Z proceed to step(83). If a waveform is present on 1/2 proceed to (81).

(80) Locate auxiliary deflection logic 2A1AlO(figure 3-3 1).

(81) Adjust 2A1A10R8 until no waveform exists with the FIELD OF VIEW switch 1A1S6 set to the 1/2 position.

(82) Disconnect TRIG IN and return to INT SYNC on scope.

(83) Set FIELD OF VIEW 1A1S6 to 1/4.

(84) Adjust 2A1A11R5 for 0.47 ± 0.01-volt peak-to-peak on oscilloscope display.

(85) Connect channel two of scope to 2A1A10J2 (red).

(86) Connect channel one of scope to 2A1XA11-14.

(87) Adjust 2A1A10R29 for 2.7 ± 0.1 volt peak-to-peak amplitude on channel two.

(88) Adjust 2A1A10R15 for 2.5 ± 0.1-volt peak-to-peak amplitude. on channel two.

(89) Adjust 2A1A10R5 for a 180° phase shift between the two sinewaves.

(90) Observe the waveform monitored CH 2 and adjust 2A1A10R28 for equal positive and negative amplitudes on .the scope.

(91) Disconnect the scope probes.

(92) Set SIM TEST/VIDEO 1A1S2 to VIDEO.

(93) Set the function generator for a sinewave; 100 kHz, 1 ± 0.1-volt peak-to-peak. Connect the output to until 1A1test point VID 1.

(94) Connect the function generator 10 nsec square-wave. output to unit 1 test point VID 2.

(95) Connect the function generator SYNC to scope TRIG IN, Adjust VIDEO IN: fully cw.

(96) Set VIDEO 2A1S2 to HS MOD.

(97) Connect the scope to VIDEO 2A1J7. Set TRIGGERING to EXT. Observe waveform AM figure 3-2.

(98) Locate write video amplifier 2A1A6 (fig. 3-4 (1)).

(99) Adjust 2A1A6R8 and 2A1A6R10 for equal chopping.

(100) Remove the scope and function generator connections.

(101) Connect the scope CH 1 to X OSC P, 2A1J18. Connect TRIG IN to 2A1A2J1 (white). Set the scope to EXT TRIG and NEG SLOPE. Observe waveform V, figure 3-2.

(102) Locate sweep and blanking 2A1A12 (fig. 3-4 (1)).

(103) Adjust 2A1A12R13 for 10 ± 0 μsec from the extreme left, beginning of the sweep to the beginning of the linear portion of the negative going sweep.

(104) Disconnect the test equipment .

(105) Remove power from the converter test set. Disconnect the cables.

(106) Return -the control units to the carrying cases (para 3-8).

3-10. Alignment

Alignment procedures are not required.

Section V. REPAIR

3-11. Parts Replacement Techniques

All parts are easily accessible and can be replaced without special procedures. The following general precautions apply to the equipment:

a. Use a pencil-type soldering iron with a 55-watt maximum capacity to prevent damage to transistors and similar components. If the iron is to be used with alternating current, use an isolating transformer between the soldering iron and the line. Do not use a soldering gun; damaging voltages can be induced in components.

b. When soldering transistor or diode leads, solder quickly; wherever wiring permits, use a heatsink (such as long-nosed pliers) between the soldered joint and the transistor or diode. Use approximately the same lead length and dress as used originally.

c. Wiring diagram information and cable diagrams in figures FO-7, 8, and 9 should be referred to as required to ensure correct part replacements.

3-12. Parts Substitution

Do not substitute parts indiscriminately. Substitute parts only when the trouble has been isolated to a specific stage and the defective part has been localized.

Section VI. GENERAL SUPPORT TEST PROCEDURES

3-13. Purpose and Instructions

a. Test procedures contained in this section are to be used for general support maintenance to determine the acceptability of repaired equipment. These procedures set forth specific requirements that repaired equipment must meet before it is returned to the using organization.

b. Perform each test in sequence; do not vary the sequence. For each step, perform all the actions required in the control settings column; then perform each specific test procedure and verify it against the performance standard.

3-14. Test equipment Required for Testing

All test equipment required to perform the testing

ing procedures of this section is listed in table 3-1.

3-15. Test Procedure

General support test procedures are contained in chart 3-3.

Chart 3.-3. General Support Test Procedure

Step no.	Control settings		Test procedure	Performance standard
	Test Equipment	Unit under test		
1	Dvm		Prepare dvm for use (para 3-3).	
2	Scope		Prepare scope for use (para 3-3).	
3	Function generator		Place jumper between 2A1J3-H and 2A1J3J.	
4		Control Unit 1A1 HORIZ SWP 1AS10: 100 KHZ OSC VERT SWP 1A1S9: CLK PULSE PWR SUP TEST 1A1S7: NOM COUNTER 1A1S11: VID GATE HOT SPOT 1A1S6: OFF VIDEO 1A1S12: VID A SUPPLY VOLTAGE 1A1SS8: 250 V FIELD OF VIEW 1A1S3: 1/4 SLEW1A1S5: 0° V/H 1A1S4: OFF BACKGND 1A1R1: CCW SIM TEST/ VIDEO 1A1S2: VIDEO 28 VDC CB1: ON 115 VAC $3_{\varnothing}$ CB2: ON Power mode switch 1A1S1: OFF LRU 1A1S13:01 Control Unit 2A1 VERT SWEEP 2A1S1: WRT COMP- SWP V HORIZ SWEEP 2A1S3: WRT SWP VIDEO 2A1S2: WRT VID SUPPLY VOLTAGE 2A1S4: 1KV VERT TEST 2A1S12: NOM RD TEST 2A1S11: NOM TUBE PROTECT/ FRAME HOLD 2A1S5: FRABME HOLD ALIGNMENT 2A1S10: OFF FOCUS TEST 2A1R23: CCW FIELD OF VIEW 2A1S6: 1/4 WRT FOCUS 2A1R2: CCW RD FOCUS 2A1R3: CCW		

Chart 3-3. General Support Test Procedure--Continued

Step no.	Control settings: Test Equipment	Control settings: Unit under test	Test procedure	Performance standard
4 contd		BACKGND 2A1R1: ccw VIDEO IN 2A1R4: ccw SLEW 2A1S7: 0° INPUTS 2A1S8: 01 LRU 2A1S9: 01		
5			Connect cable W3 between unit under test unit 1, 1A1J3; and unit 2, 1A1J1. Connect cables W1 and W2 to ac and de power sources.	
		Power mode switch 1A1S1: STBY		STBY lamp lights. No other lamps light.
		Power mode switch 1A1S1: OPR		STBY lamp extinguishes. OPR lamp lights. No other lamp lights.
8	Dvm		Perform voltage measurements (table 3-2, items 1 through 38).	Observe dvm indication.
9	Dvm		Check resistance values (table 3-3; items 1 through 3).	Observe dvm indication.
10	Dvm		Check continuity (table 3-4, items 1 through 220).	Observe dvm indication.
11	Scope: TIME/CM: 1 ms VOLTS/CM: 2.o		Connect scope GND to unit 1A1 GND; connect probe to 1A 1J7-H.	Observe waveform A, figure 3-2.
12			Move scope probe to 1AIJ7J.	Observe waveform B, figure 3-2.
13	TIME/CM:5,µs		Move scope probe to test point TEST 4.	Observe waveform C, figure 3-2.
14	VOLTS/CM:0.5	VIDEO/SIM TEST 1A1S2: SIM TEST	Move scope probe to test point TEST 7.	Observe waveform D, figure 3-2.
15			Move scope probe to test point TEST 8.	Observe waveform E, figure 3-2.
16	VOLTS/CM:1.0	VIDEO/SIM TEST 1AS2: VIDEO	Move scope probe to test point 9.	Observe waveform F, figure 3-2.
17			Move scope probe to test point CTR (J1).	Observe waveform G, figure 3-2.
18		HOT SPOT 1A1S6: ON	Move scope probe to test point TEST 6.	Observe waveform H, figure 3-2.
19			Move scope probe to test point TEST 5.	Observe waveform I, figure 3-2.
20			Move scope probe to 1A1J7-M.	Observe waveform J, figure 3-2.
21	TIME/CM: 5µs VOLTS/CM:0.1	HOT SPOT 1A1S6: OFF COUNTER A1S11: 100 KHZ OSC	Move scope probe to test point CRT.	Observe waveform K, figure 3-2.
22		HORIZ SWEEP 2A1S3: RD HORIZ SYNC	Move scone probe to test point HORIZ SWP unit 2.	Observe waveform L, figure 3-2.
23		VERT SWEEP 2A1S1: RD SWP V	Move scope probe to test point VERT SWP unit 2.	Observe waveform M, figure 3-2.
24	TIME/CM: 1 ms VOLTS/CGM: 2	HORIZ SWEEP 2A1S3: WRT SWP SLEW 2A1S7: 0' FIELD OF VIEW 2A1S6: FULL	Move scope probe to test point HORIZ SWP unit 2.	Observe waveform N, figure 3-2.
25		SLEW 2A1S7: 0 FIELD OF VIEW 2A1S6: 1/2		Observe waveform 0, figure 3-2.
26		SLEW 2A1S7: LEFT 30' FIELD OF VIEW 2A1S6: 1/4		Observe waveform P, figure 3-2.

Chart 3-3. General Support Test Procedure-Continued

Step no.	Control settings: Test Equipment	Control settings: Unit under test	Test procedure	Performance standard
27		SLEW 2A1S7: RIGHT 30°	•	Observe waveform Q, figure 3-2.
28	TIME/CM:1 ms VOLTS/CM: 1	FIELD OF VIEW 2A1S6; FULL	Move scope probe to test point INPUT C.	Observe waveform R, figure 3-2.
29		VIDEO 2A1S2: HS MOD	a. Move scope probe to test point VIDEO, Adjust; VIDEO IN fully cw. b. Adjust VIDEO IN fully CCW.	a. Observe waveform S, figure 32. b. Amplitude of waveform <0.5 V.
30		VIDEO IN 2A1R4: CW VERT SWEEP 2A1S1: WRT COMP SWP V TUBE PROTECT/ FRAME HOLD: TUBE PROTECT	Move scope probe to test point VERT SWP.	Observe waveform T, figure 3-2.
31	VOLTS/ CM: .1		Move scope probe to 2A1J4-c.	Observe waveform U, figure 3-2.
32	VOLTS/CM: 1.0 TIME/CM: 51s.		Move scope probe to test point X OSCP.	Observe waveform V, figure 3-2.
33			Move scope probe to test point Y OSCP.	Observe waveform W, figure 3-2.
34	Function generator		a. Insert 100 kHz at 2A1J2-e. b. Move scope probe to test point Z OSCP. c. Sync scope at Y OSCP on unit 2.	a. None. b. Observe waveform X, figure 3-2.

APPENDIX A
REFERENCES

DA Pam 310-1	Consolidated Index of Army Publications and Blank Forms.
TM 11-5850-241-34/1	Direct Support and General Support Maintenance Manual: Detecting Set Infrared AN/AAS-24 (NSN 5850-00-179-8429) (Vol. 1 of 2).
TM 11-5850-241-34/2	(C) DS and GS Maintenance Manual for Detecting Set, Infrared AN/AAS-24(U) (Vol. 2 of 2).
TM 11-6625-366-15	Operator's, Organizational, Direct Support, General Support and Depot Maintenance Manual: Multimeter TS-352B/U (NSN 6625-00-553-0142).
TM 11-6625-1703-15	Operator's, Organizational, Direct Support, General Support and Depot Maintenance Manual: Oscilloscope AN/USM-281A(NSN 6625-00-228-2201).
TM 11-6625-1732-12	Operator's and Organizational Maintenance Manual (Including Repair Parts and Special Tools List): Test Set, Resolution AN/AAM-30 (NSN 6625-00-433-2415); Cable Assembly Set, Electrical MX-8408 /AAS-24 (6625-00-489-0468); Maintenance Kit, Electronic Equipment MK-1172/AAS-24 (5850-00-434-5539) and Fixture, Alignment MX-8409/AAS-24 (6625-00-489-2673).
TM 11-6625-1824-12	Operator's and Organizational Maintenance Manual (Including Repair Parts and Special Tool List): Test Set, Converter Subassembly-Video Converter AN/AAM-35 (NSN 6625-00-403-1064).
TB SIG 222	Solder and Soldering.

By Order of the Secretary of the Army:

W. C. WESTMORELAND,
General, United States Army,
***Chief of Staff*.**

Official:

KENNETH G. WICKHAM,
Major General, United States Army,
The Adjutant General.

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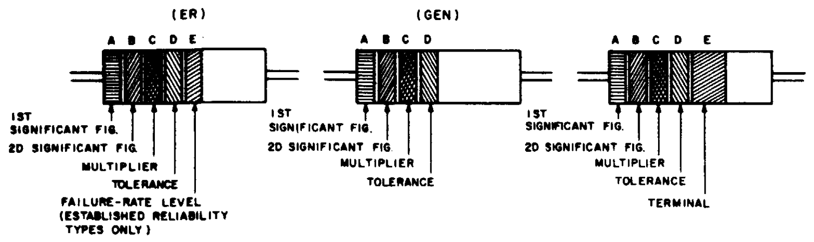


COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS.

COLOR-CODE MARKING FOR FILM-TYPE RESISTORS.

TABLE I
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS

BAND A		BAND B		BAND C		BAND D		BAND E		
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL	TERM.
BLACK	0	BLACK	0	BLACK	1			BROWN	M	
BROWN	1	BROWN	1	BROWN	10			RED	P	
RED	2	RED	2	RED	100			ORANGE	R	
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S	
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP. TYPE ONLY)	WHITE		SOLD-ERABLE
GREEN	5	GREEN	5	GREEN	100,000	GOLD	±5			
BLUE	6	BLUE	6	BLUE	1,000,000	RED	±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY).			
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7							
GRAY	8	GRAY	8	SILVER	1.01					
WHITE	9	WHITE	9	GOLD	0.1					

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH.)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE.

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)

BAND D — THE RESISTANCE TOLERANCE.

BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE-RATE LEVEL. ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1-1/2 TIMES THE WIDTH OF OTHER BANDS, AND INDICATES TYPE OF TERMINAL.

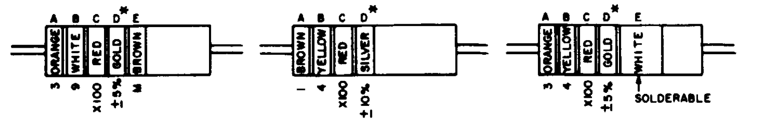
RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS
(THESE ARE NOT COLOR CODED)

SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE:

2R7 = 2.7 OHMS   10R0 = 10.0 OHMS

FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED. IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS.

EXAMPLES OF COLOR CODING



NOMINAL RESISTANCE 3,900 OHMS
RESISTANCE TOLERANCE ±5%
FAILURE RATE LEVEL M

NOMINAL RESISTANCE 1,400 OHMS
RESISTANCE TOLERANCE ±10%

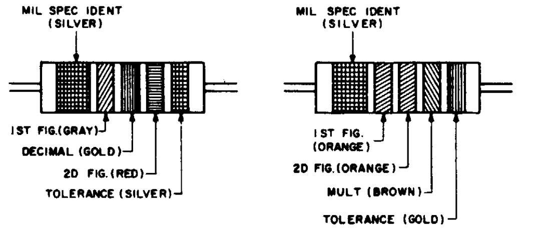
NOMINAL RESISTANCE 3,400 OHMS
RESISTANCE TOLERANCE ±5%
TERMINAL SOLDERABLE

COMPOSITION-TYPE RESISTORS

FILM-TYPE RESISTORS

* IF BAND D IS OMITTED, THE RESISTOR TOLERANCE IS ±20% AND THE RESISTOR IS NOT MIL-STD.

A. COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS.



(A) 8.2UH ± 10%

(B) 330UH ± 5%

COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES. AT A, AN EXAMPLE OF OF THE CODING FOR AN 8.2UH CHOKE IS GIVEN. AT B, THE COLOR BANDS FOR A 330UH INDUCTOR ARE ILLUSTRATED.

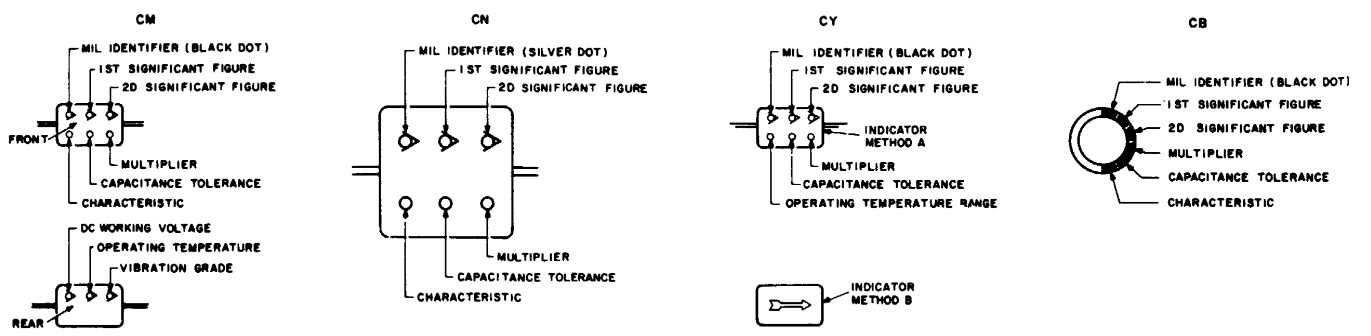
TABLE 2
COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES.

COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN	1	10	1
RED	2	100	2
ORANGE	3	1,000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD	DECIMAL POINT		5

MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL.

B. COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS.

CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CY, AND CB.

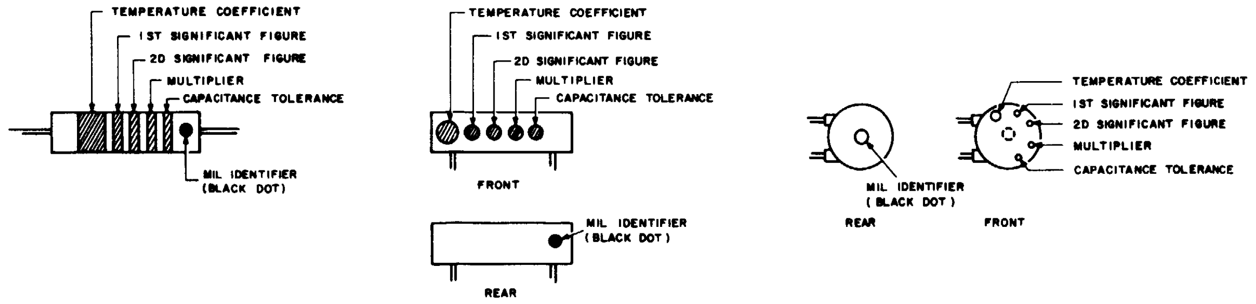


MICA-DIELECTRIC

PAPER-DIELECTRIC

GLASS-DIELECTRIC, GLASS CASE

MICA, BUTTON TYPE



AXIAL LEAD

RADIAL LEAD

DISK-TYPE

TABLE 3 — FOR USE WITH STYLES CM, CN, CY AND CB.

COLOR	MIL ID	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER[1]	CAPACITANCE TOLERANCE				CHARACTERISTIC[2]			DC WORKING VOLTAGE	OPERATING TEMP. RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CB	CM	CY, CM	CM
BLACK	CM, CY CB	0	0	1			±20%	±20%		A			-55° TO +70°C	10-55 HZ
BROWN		1	1	10					B	E	B			
RED		2	2	100	±2%		±2%	±2%	C				-55° TO +85°C	
ORANGE		3	3	1,000		±30%			D		D	300		
YELLOW		4	4	10,000					E				-55° TO +125°C	10-2,000HZ
GREEN		5	5		±5%				F			500		
BLUE		6	6										-55° TO +150°C	
PURPLE (VIOLET)		7	7											
GREY		8	8											
WHITE		9	9											
GOLD				0.1			±5%	±5%						
SILVER	CN				±10%	±10%	±10%	±10%						

TABLE 4 — TEMPERATURE COMPENSATING, STYLE CC.

COLOR	TEMPERATURE COEFFICIENT[4]	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER[1]	CAPACITANCE TOLERANCE		MIL ID
					CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	
BLACK	0	0	0	1		±2.0 UUF	CC
BROWN	-30	1	1	10	±1%		
RED	-80	2	2	100	±2%	±0.25 UUF	
ORANGE	-150	3	3	1,000			
YELLOW	-220	4	4				
GREEN	-330	5	5		±5%	±0.5 UUF	
BLUE	-470	6	6				
PURPLE (VIOLET)	-750	7	7				
GREY		8	8	0.01			
WHITE		9	9	0.1	±10%		
GOLD	+100					±1.0 UUF	
SILVER							

1. THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF.

2. LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS: MIL-C-5, MIL-C-25D, MIL-C-11272B, AND MIL-C-10950C RESPECTIVELY.

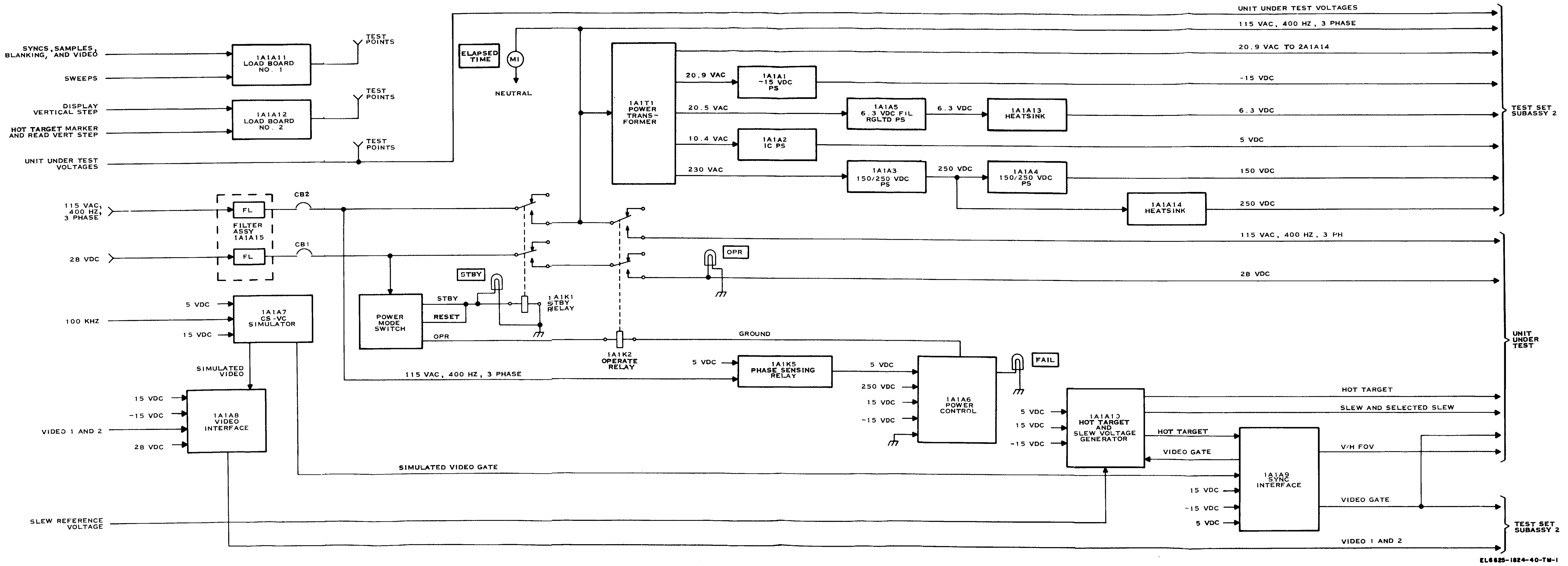
3. LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D.

4. TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE.

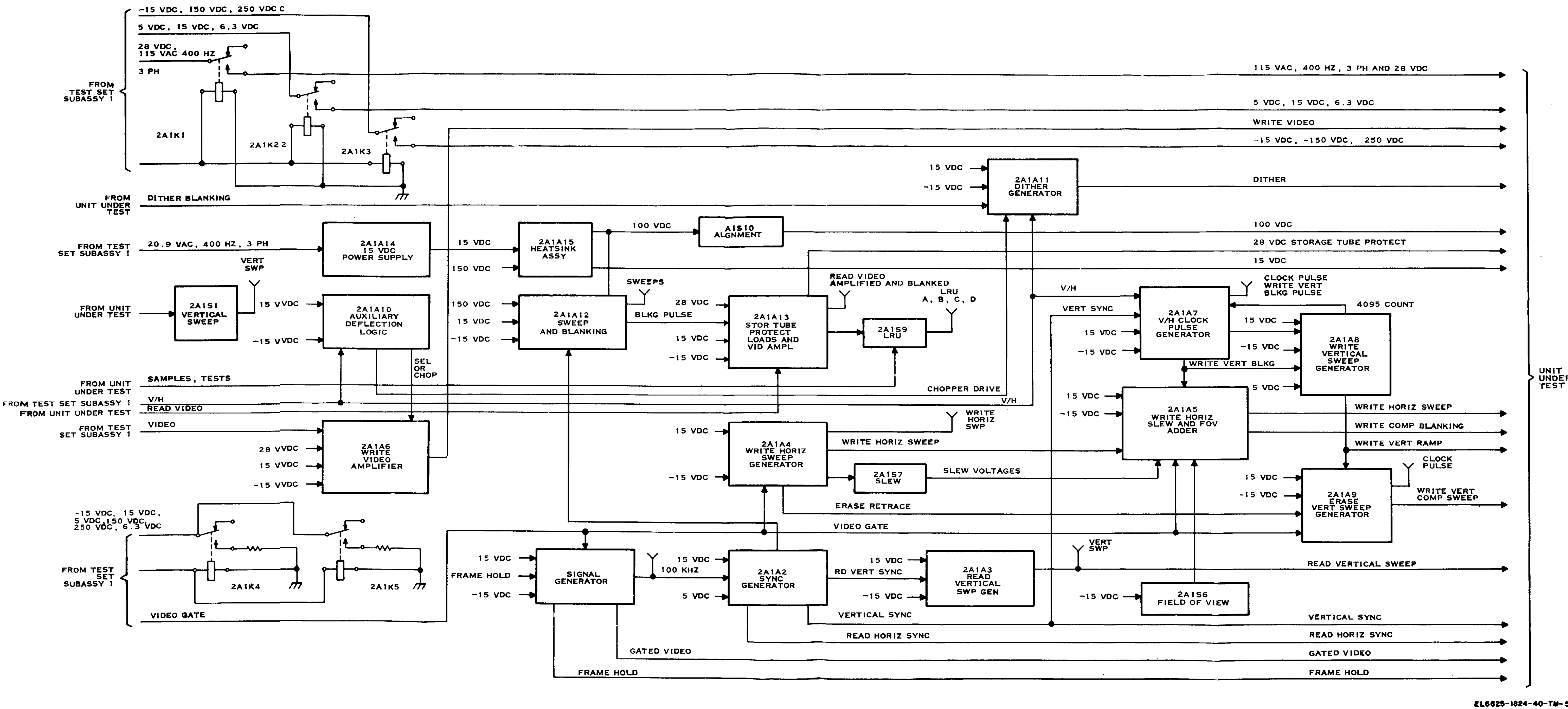
C. COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS.

ESC-FM 4118-69

FO-1. Color code for military standard resistors, inductors and capacitors.



FO-2. Block diagram, control unit 1A1.



FO-3. Block diagram, control unit 2A1.

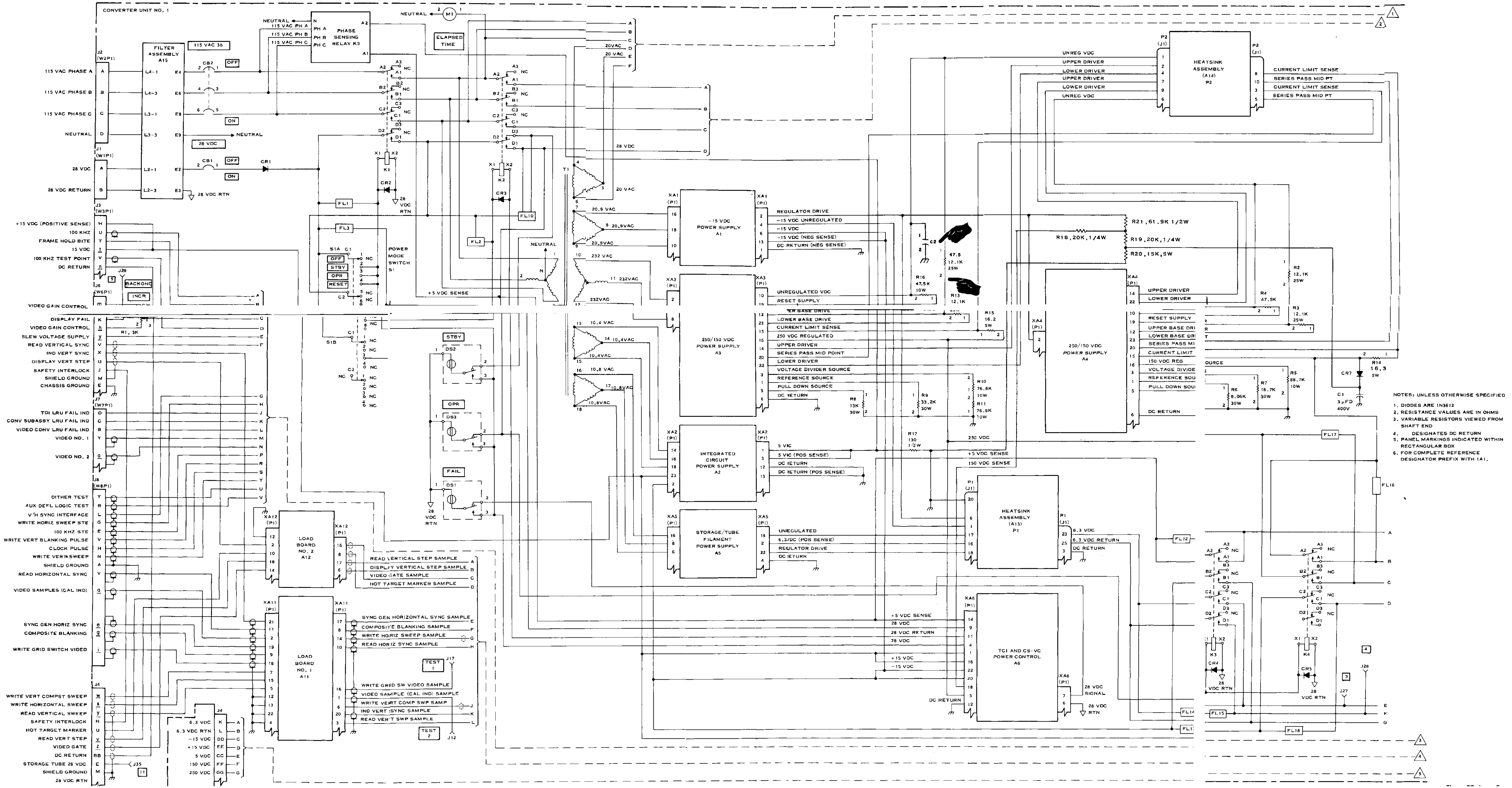
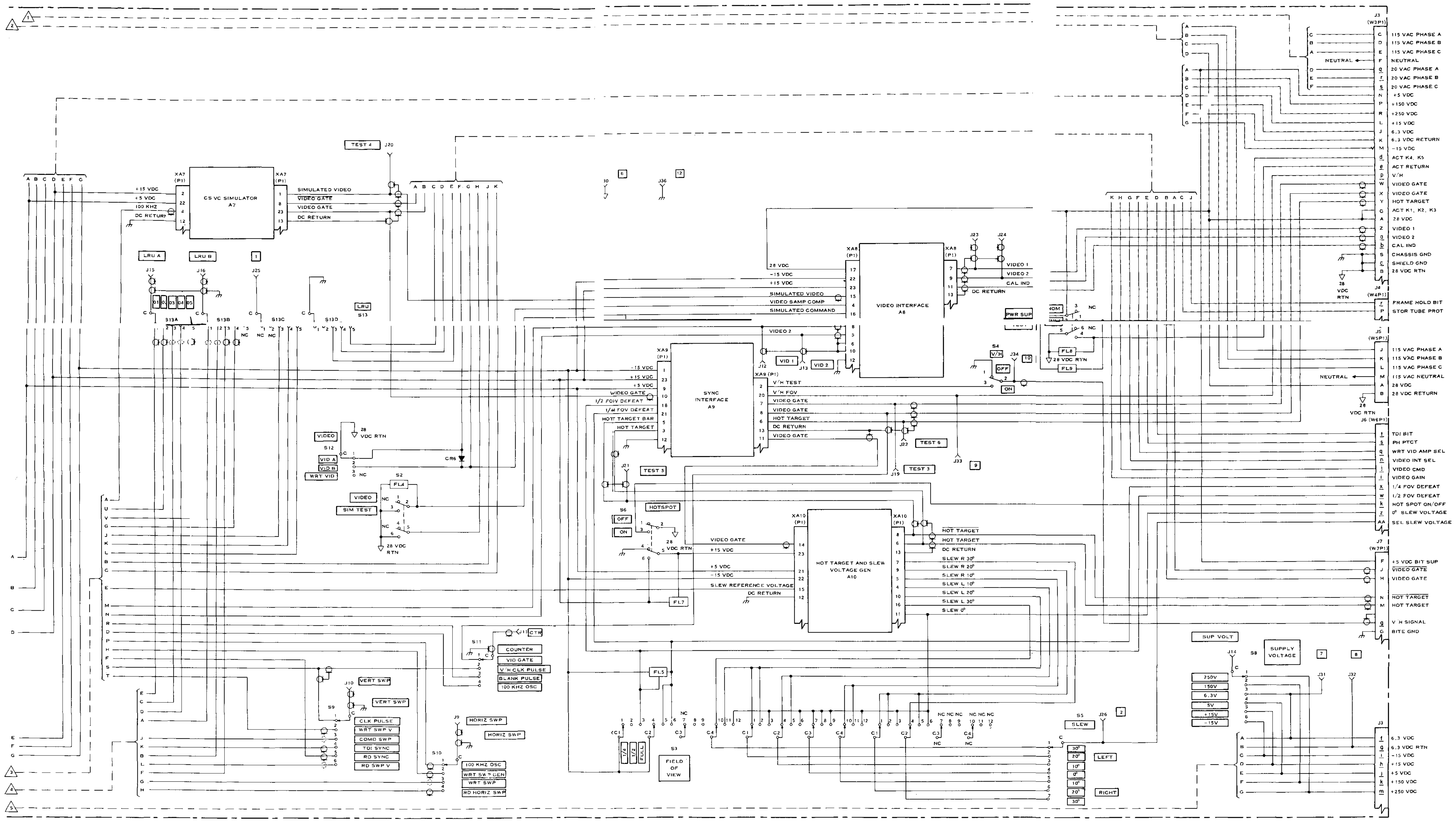


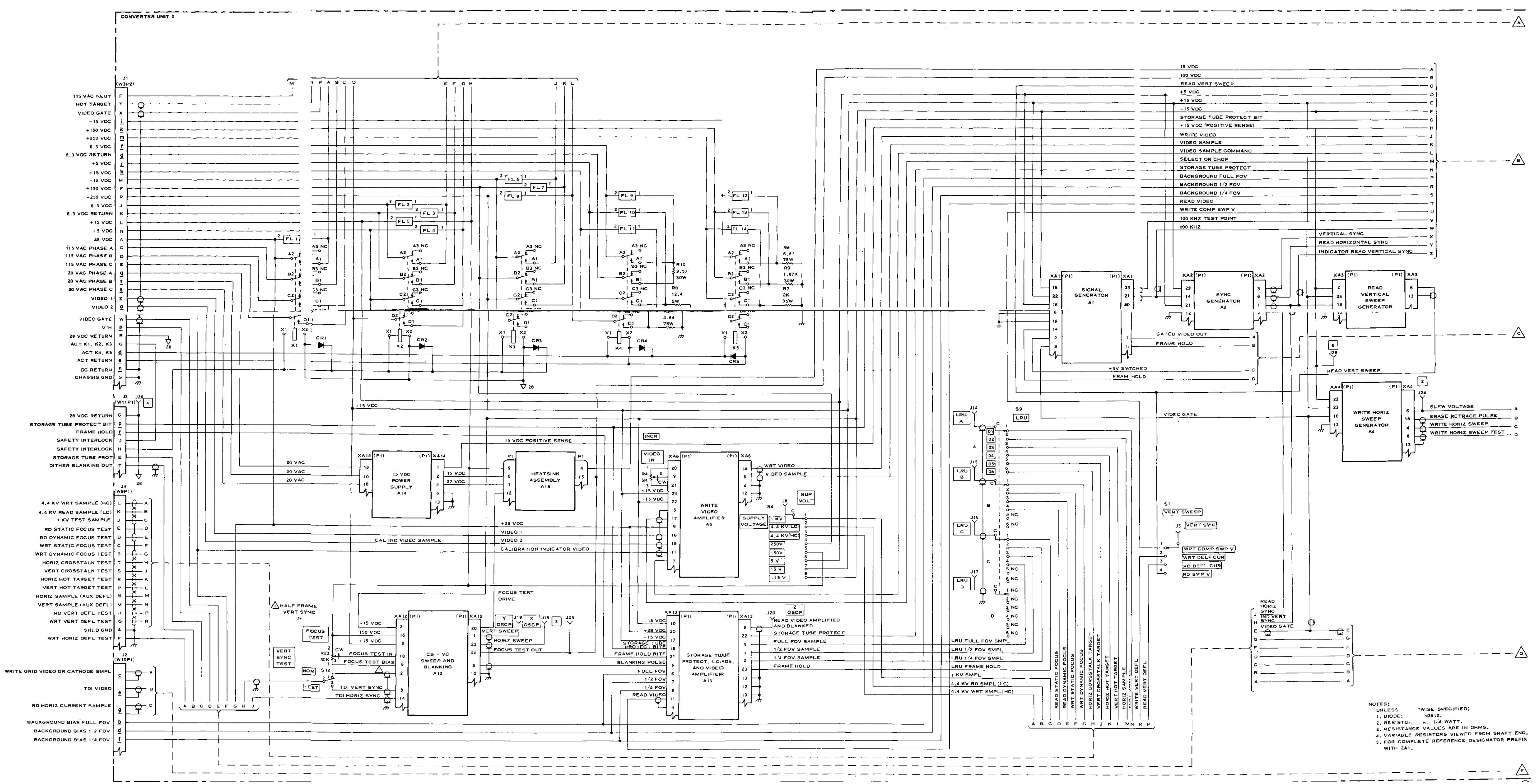
Figure FO-4. Overall Schematic Diagram, Control Unit 1A1 (Part 1 of 4).

EL4IM011



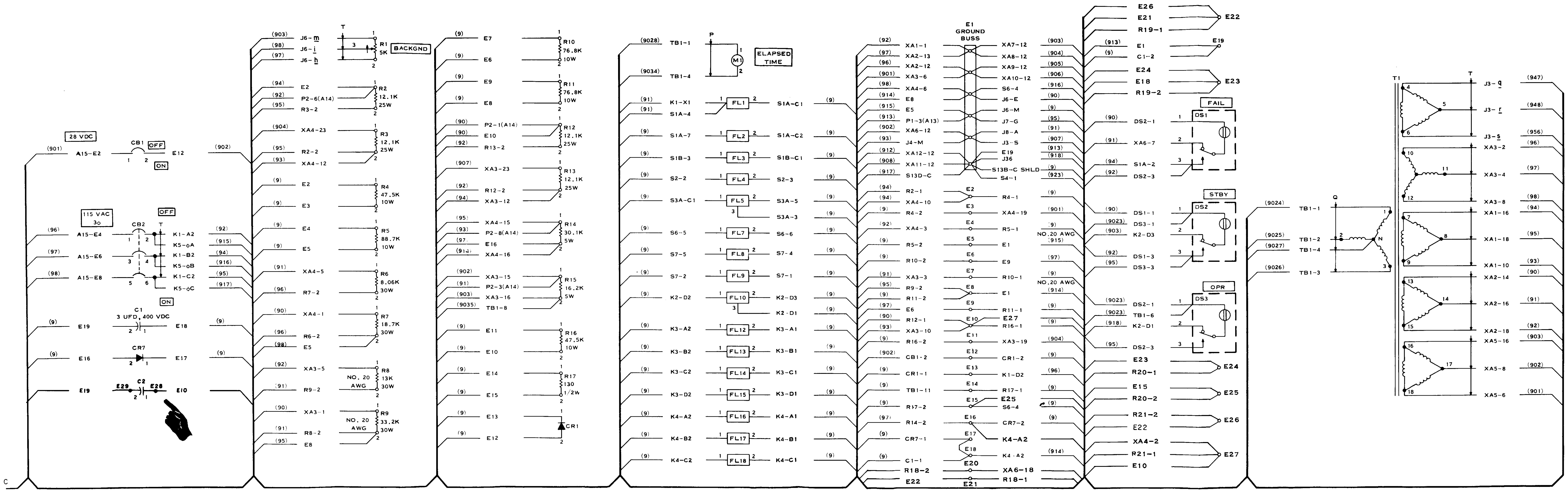
FO-4(2). Overall schematic diagram, control unit 1a1 (part 2 of 2).

EL6625-1824-40-TM-59(2)



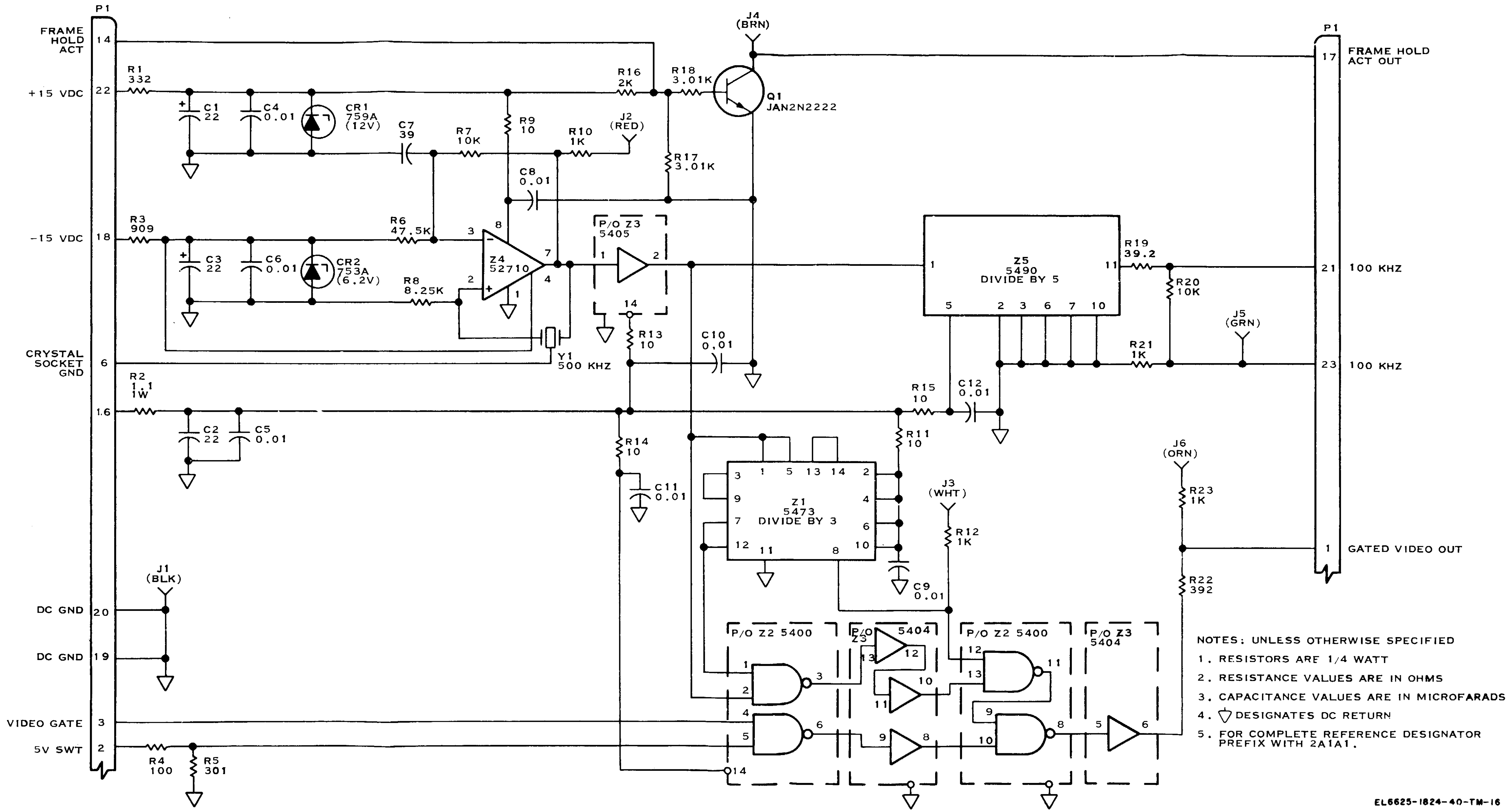
FO-5(1). Overall schematic diagram, control unit 2A1 (part 1 of 2).

EL6625-1824-40-TM-61(1)

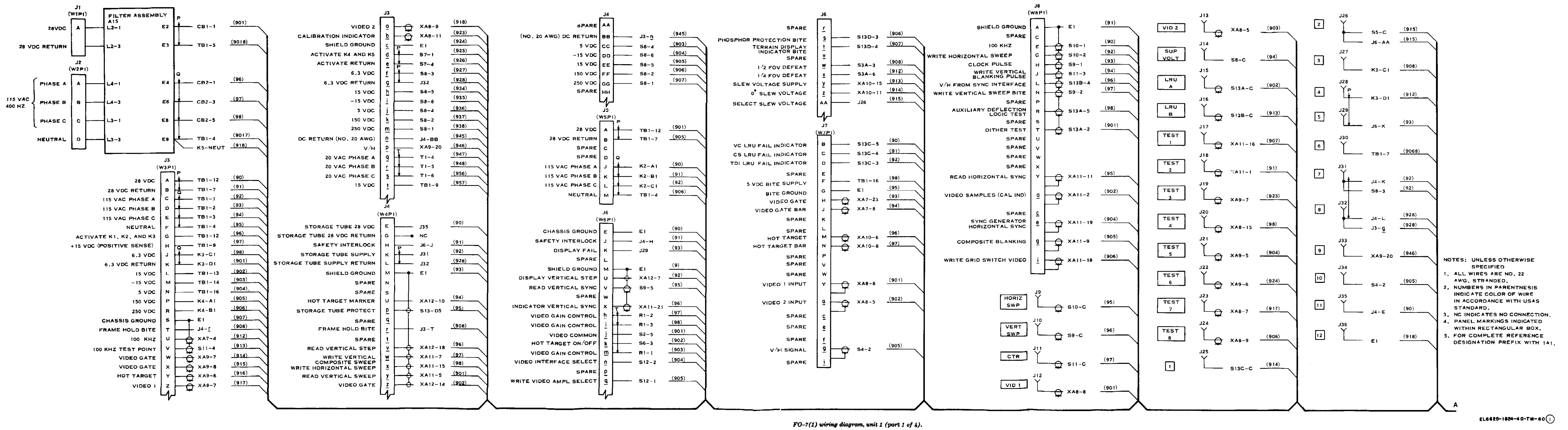


EL4IM012

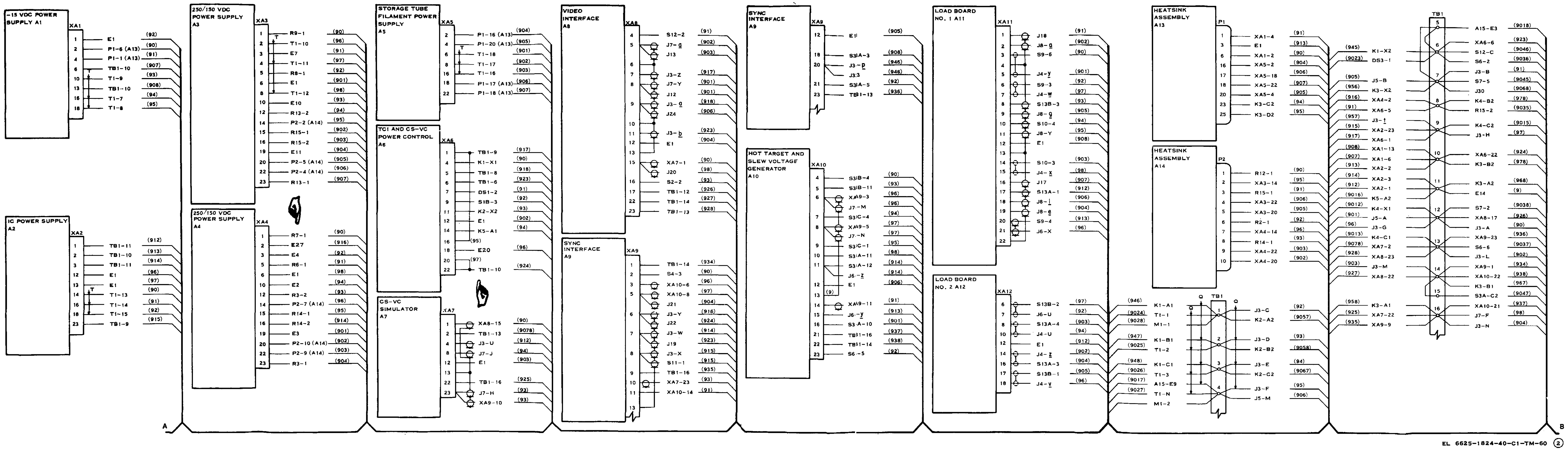
Figure FO-7 . Wiring Diagram, Unit 1 (Part 4 of 4).



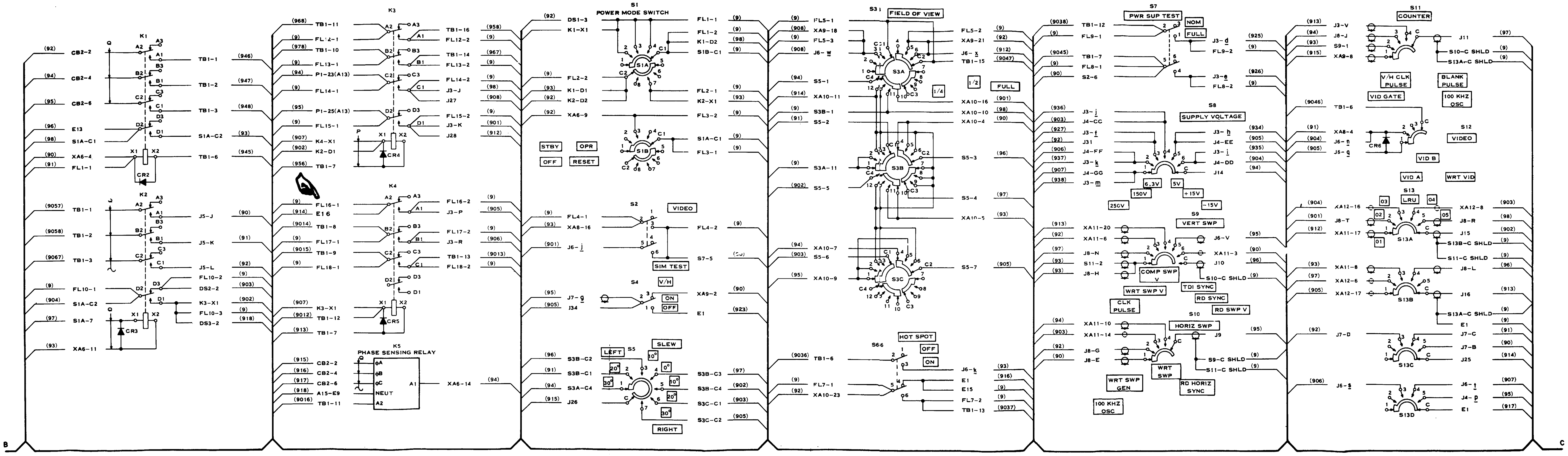
FO-6. Signal generator 2A1A1, schematic diagram.



FO-7(1) wiring diagram, unit 1 (part 1 of 4).

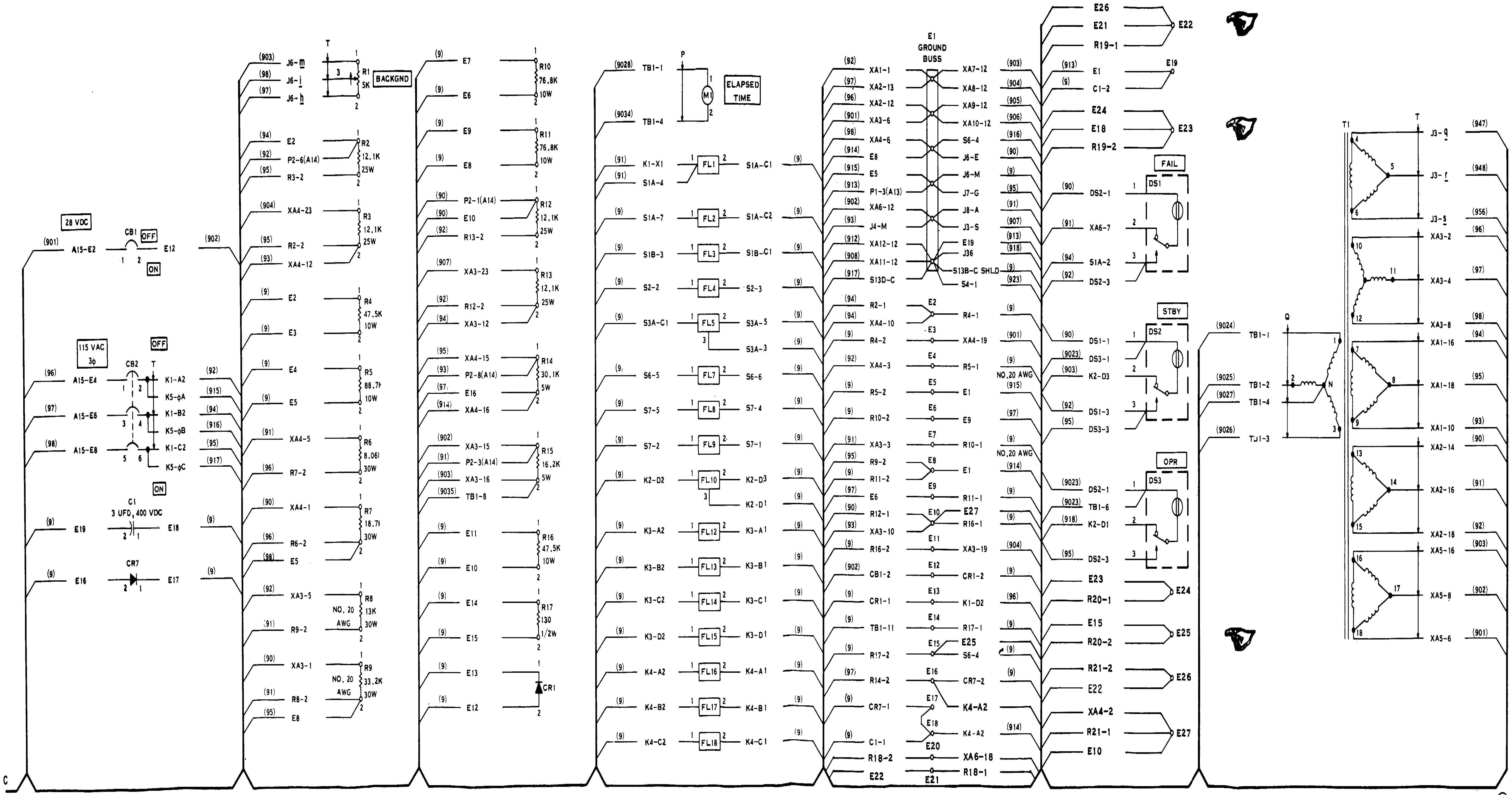


FO-7(2). Wiring diagram, unit 1 (part 2 of 4).



EL 6625-1824-40-C1-TM-60 (3)

FO-7(3). Wiring diagram, unit 1 (part 3 of 4).



EL 6625-1824-40-C1-TM-60 (4)

Figure FO-7 (4). Wiring Diagram, unit 1 (part 4 of 4)

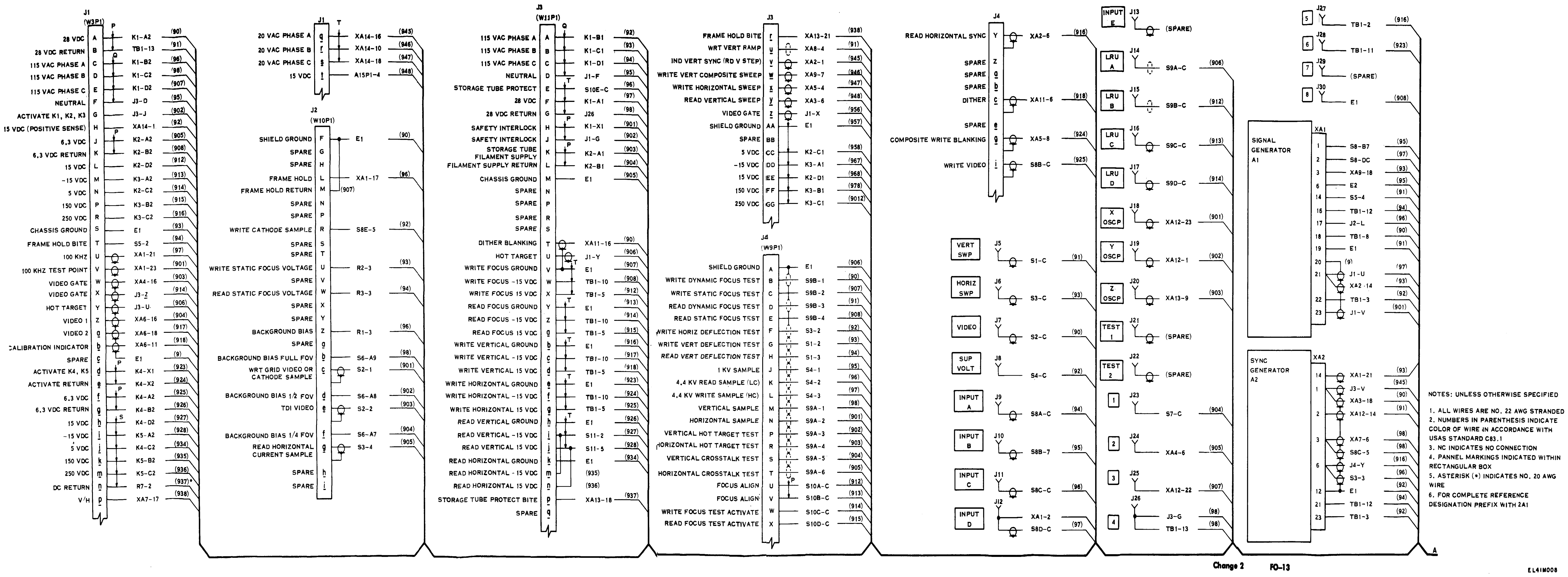


Figure FO-8(1). Wiring Diagram, unit 2 (part 1 of 4)

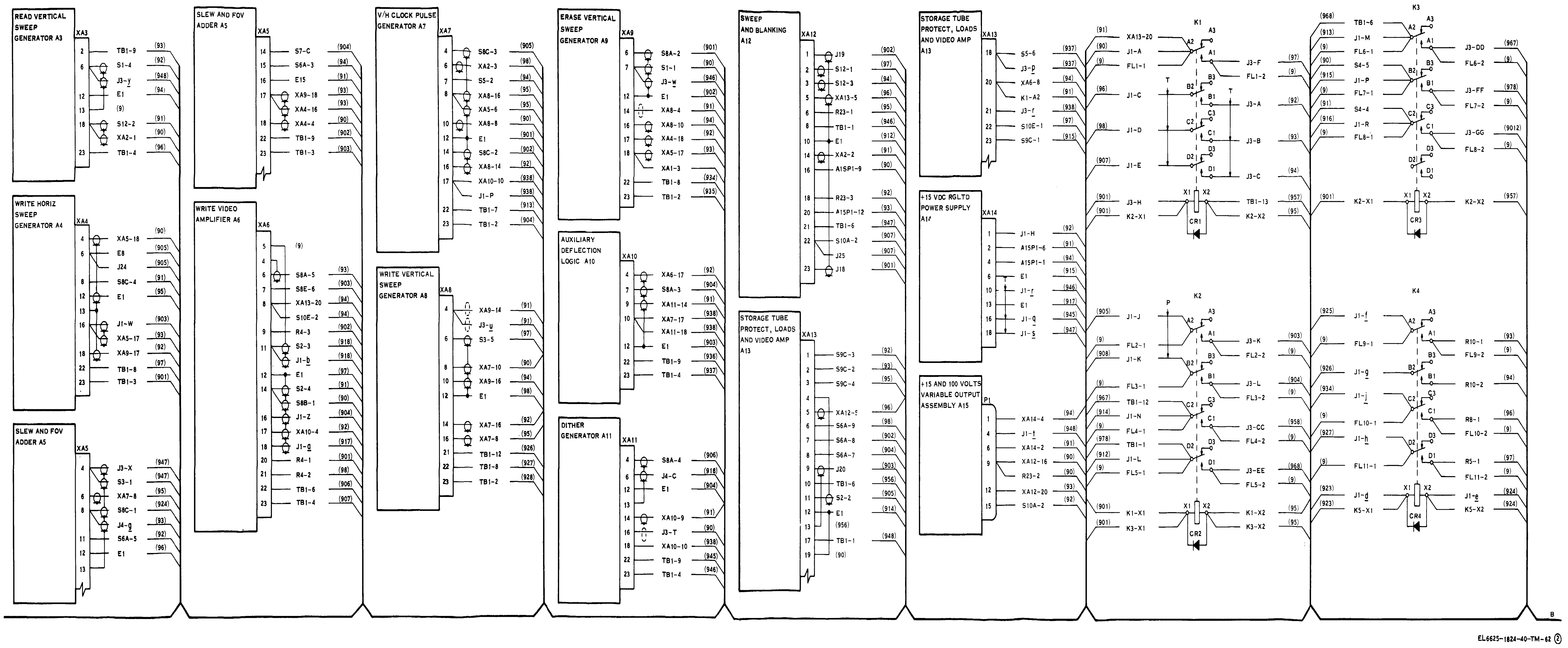


Figure FO-8(2). Wiring Diagram, unit 2 (part 2 of 4)

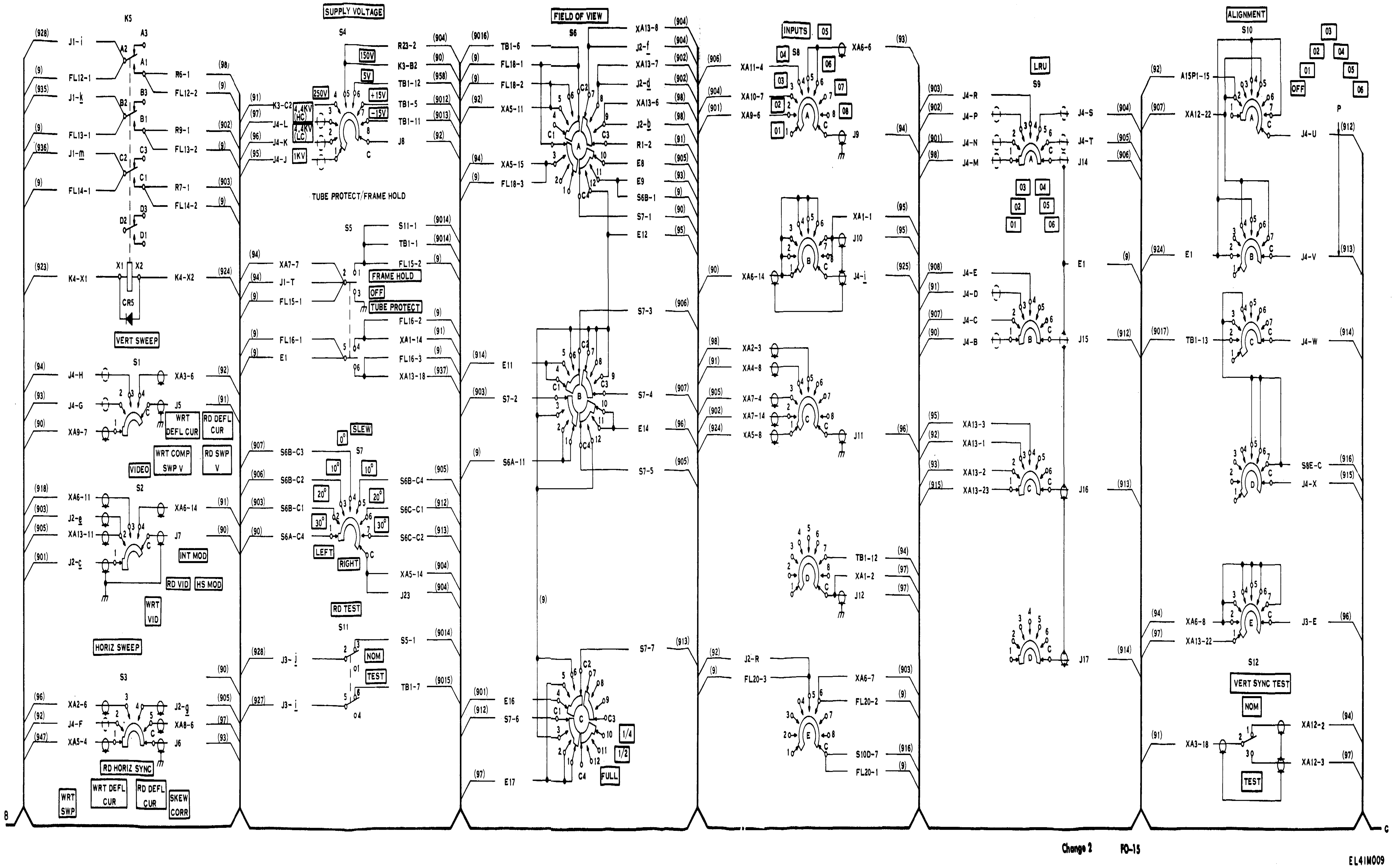


Figure FO-8(3). Wiring Diagram, unit 2 (part 3 of 4)

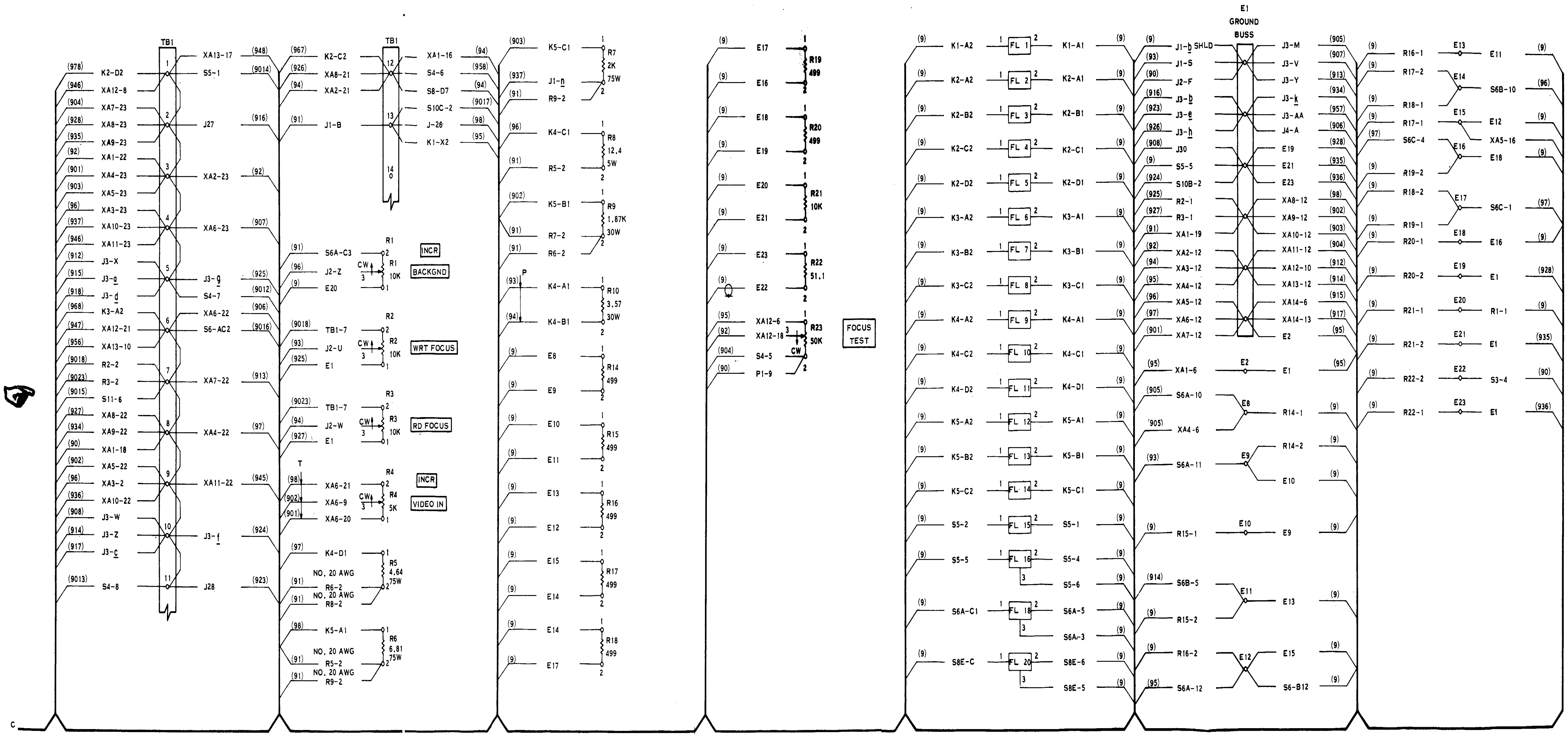
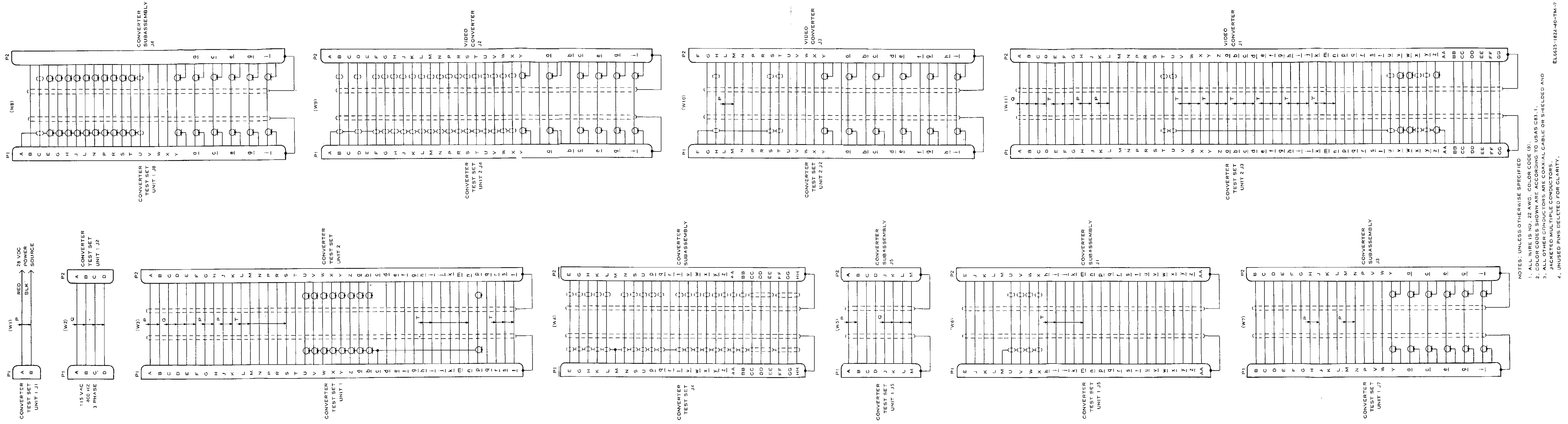


Figure FO-8. Wiring diagram, unit 2 (part 4 of 4).

Change 2 FO-16

EL41M007

Figure FO-8(4). Wiring diagram, unit 2 (part 4 of 4).



FO-9. Cable Diagram.

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

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PUBLICATION NUMBER	PUBLICATION DATE	PUBLICATION TITLE

BE EXACT PIN-POINT WHERE IT IS				IN THIS SPACE, TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT.
PAGE NO.	PARA-GRAPH	FIGURE NO.	TABLE NO.	

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DA FORM 1 JUL 79 2028-2

PREVIOUS EDITIONS ARE OBSOLETE.

P.S.--IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR RECOMMENDATION MAKE A CARBON COPY OF THIS AND GIVE IT TO YOUR HEADQUARTERS.

The Metric System and Equivalents

Linear Measure

1 centimeter = 10 millimeters = .39 inch
1 decimeter = 10 centimeters = 3.94 inches
1 meter = 10 decimeters = 39.37 inches
1 dekameter = 10 meters = 32.8 feet
1 hectometer = 10 dekameters = 328.08 feet
1 kilometer = 10 hectometers = 3,280.8 feet

Weights

1 centigram = 10 milligrams = .15 grain
1 decigram = 10 centigrams = 1.54 grains
1 gram = 10 decigram = .035 ounce
1 decagram = 10 grams = .35 ounce
1 hectogram = 10 decagrams = 3.52 ounces
1 kilogram = 10 hectograms = 2.2 pounds
1 quintal = 100 kilograms = 220.46 pounds
1 metric ton = 10 quintals = 1.1 short tons

Liquid Measure

1 centiliter = 10 milliters = .34 fl. ounce
1 deciliter = 10 centiliters = 3.38 fl. ounces
1 liter = 10 deciliters = 33.81 fl. ounces
1 dekaliter = 10 liters = 2.64 gallons
1 hectoliter = 10 dekaliters = 26.42 gallons
1 kiloliter = 10 hectoliters = 264.18 gallons

Square Measure

1 sq. centimeter = 100 sq. millimeters = .155 sq. inch
1 sq. decimeter = 100 sq. centimeters = 15.5 sq. inches
1 sq. meter (centare) = 100 sq. decimeters = 10.76 sq. feet
1 sq. dekameter (are) = 100 sq. meters = 1,076.4 sq. feet
1 sq. hectometer (hectare) = 100 sq. dekameters = 2.47 acres
1 sq. kilometer = 100 sq. hectometers = .386 sq. mile

Cubic Measure

1 cu. centimeter = 1000 cu. millimeters = .06 cu. inch
1 cu. decimeter = 1000 cu. centimeters = 61.02 cu. inches
1 cu. meter = 1000 cu. decimeters = 35.31 cu. feet

Approximate Conversion Factors

To change	*To*	*Multiply by*	*To change*	*To*	*Multiply by*
inches	centimeters	2.540	ounce-inches	Newton-meters	.007062
feet	meters	.305	centimeters	inches	.394
yards	meters	.914	meters	feet	3.280
miles	kilometers	1.609	meters	yards	1.094
square inches	square centimeters	6.451	kilometers	miles	.621
square feet	square meters	.093	square centimeters	square inches	.155
square yards	square meters	.836	square meters	square feet	10.764
square miles	square kilometers	2.590	square meters	square yards	1.196
acres	square hectometers	.405	square kilometers	square miles	.386
cubic feet	cubic meters	.028	square hectometers	acres	2.471
cubic yards	cubic meters	.765	cubic meters	cubic feet	35.315
fluid ounces	milliliters	29,573	cubic meters	cubic yards	1.308
pints	liters	.473	milliliters	fluid ounces	.034
quarts	liters	.946	liters	pints	2.113
gallons	liters	3.785	liters	quarts	1.057
ounces	grams	28.349	liters	gallons	.264
pounds	kilograms	.454	grams	ounces	.035
short tons	metric tons	.907	kilograms	pounds	2.205
pound-feet	Newton-meters	1.356	metric tons	short tons	1.102
pound-inches	Newton-meters	.11296			

Temperature (Exact)

°F	Fahrenheit temperature	5/9 (after subtracting 32)	Celsius temperature	°C

PIN: 017557-000